MB211S IDTV
SERVICE MANUAL

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1. INTRODUCTION

17MB211 main board is driven by Novatek SOC. This IC is a single chip iDTV solution which compliants with variety ATV as NTSC, PAL and SECAM, and DTV standards as ISDB-T, DVB-T/-T2/-C/-S/-S2, ITU-T J.83B, ATSC, integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing.

Key features include:

- ATSC,DVB-T,T2,DVB-C, DVB-S/S2 demodulators
- A multi standart A/V format decoder
- Advanced Super Resolution 5th generation Advanced Scaling Up Engine
- Embedded dual 10 bit LVDS transmitter
- Dedicated DSP to decode compressed audio
- 4K2K 30p HDMI input with scaling down
- Rich internet connectivity and completed digital home network solution
- Mılti-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM

Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Side AV (CVBS, R/L_Audio)
- 1 BAV-IN socket(Common)
- 1 PC input(Common)
- 3 HDMI input
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(1x common, 1x optional) and 2x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 External Touchpad/ Keyboard/Magic Button
- 1 DVD(Optional)

2. T/T2/C/A TUNER (U1)

Description

The MxL661 is a highly integrated low-power silicon tuner IC that targets all global and digital cable standards. Broadband input filtering and channel filtering have been completely integrated on-chip. This integration enables a compact design resulting in small footprint, low Bill-Of-Material (BOM) cost, and low-power consumption.

A signal at the 75ohm RF input is filtered and converted to a programmable IF output frequency. Automatic Gain Control (AGC), LO generation, and channel selectivity functions are completey integrated on the chip. All functions of the IC can be controlled using the I2C interface.

The MxL is available in a 4 mm x 4mm x 0.85mm3, 24-pin QFN package.

Features

- Tuning range from 44MHz to 1002MHz
- Programmable channel bandwidths of 6, 7, and 8MHz
- Integrated channel filtering
- Low power consumption with 3.3V and 1.8V dual-supply operation - 351 mW (digital terrestrial)
- On-chip voltage regulator enables single supply 3.3V operation
- Programmable IF frequency and IF spectrum inversion
- Programmable RF to IF delay for ATV scrambling systems that relies on the H-Sync method
- Optioanl balun-less application note for cost-sensitive applications
- Reference clock output available for re-use by demodulators and additional tuners in multi-channel applications
- Input power reporting
- Open-drain General Purpose Output GPO available for controlling off-chip circuitry
- I^2C compatible digital control interface
- RoHS compliance

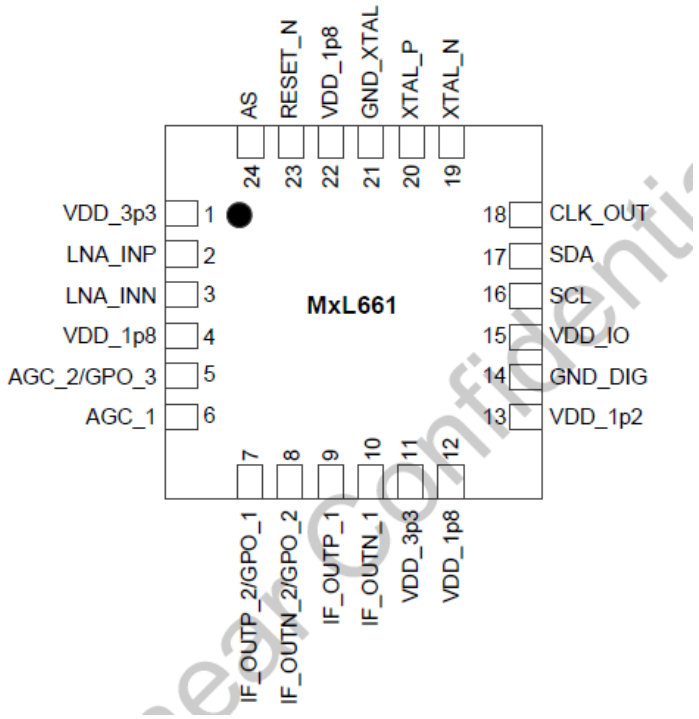

Figure: Pin description

Pin #	Pin Name
1	VDD_3p3
2	LNA_INP
3	LNA_INN
4	VDD_1p8
5	AGC_2/GPO_3
6	AGC_1
7	IF_OUTP_2/GPO_1
8	IF_OUTN_2/GPO_2
9	IF_OUTP_1
10	IF_OUTN_1
11	VDD_3p3
12	VDD_1p8

Pin #	Pin Name
13	VDD_1p2
14	GND_DIG
15	VDD_IO
16	SCL
17	SDA
18	CLK_OUT
19	XTAL_N
20	XTAL_P
21	GND_XTAL
22	VDD_1p8
23	RESET_N
24	AS

Table: Pin functions

3. S/S2 TUNER (U142)

Description

The AV2018 is a highly integrated silicon tuner for DVB-S2 standard. It integrates a synthesizer, crystal oscillator, LDO, loop through path, and a direct conversion receiver including LNA, RF variable gain amplifiers, Mixer, programmable channel filter, and PGA.

The low noise figure of the receiver and loop through path eliminates the need of an external LNA. The integrated crystal oscillator can provide a reference clock for demodulator. The LDO supplies all the internal blocks the only an external voltage source is required. The AV2018 requires only a small number of external components, thus enables very competitive design.

The AV2018 implements an automatic gain control mechanism that only an analog control signal from the demodulator is required to from a close-loop gain control. The mechanism will arrange the gain of the receiver

blocks to achieve best performance according to the control signal voltage. The embedded automatic calibration mechanism provides precise control of channel filter bandwidth and DC offset, no additional calibration procedure is required.

Features

- Input RF Frequency: 950Mhz to 2150Mhz
- Single +3.3V power Supply
- Embedded LNA, Mixer, VCO, crystal oscillator, and LDO
- Low Noise Figure: 5 dB, typical
- Embedded DC offset Cancellation Circuit
- Programmable channel filter with bandwith from 4MHz to 40MHz
- Automatic gain control
- Embedded RF signal loop through path
- Single-ended I/Q interface
- QFN3*3mm 16pin package

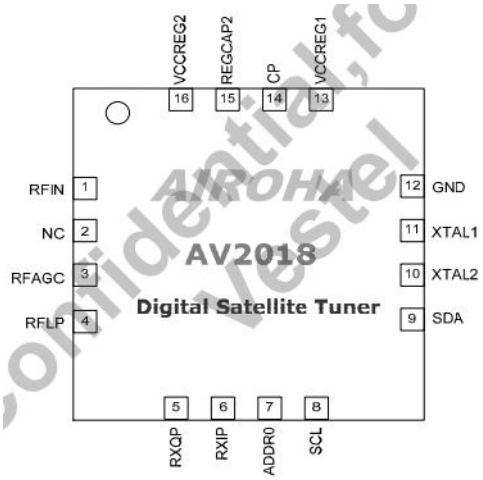

Figure 3: Pin Assigment

PIN	SIGANL	TYPE	DESCRIPTION
1	RFIN	Input, Analog	RF Signal Input
2	NC	-	No Connect
3	RFAGC	Input, Analog Control	RF AGC Control Voltage
4	RFLP	Output, Analog	RF Loop Through Signal Output
5	RXQP	Output, Analog	BB Output
6	RXIP	Output, Analog	BB Output
7	ADDR0	Digital	Device Address Control
8	SCL	Input, Digital	Serial Interface
9	SDA	Input/Output, Digital	Serial Interface
10	XTAL2	Analog	XTAL Input
11	XTAL1	Analog	XTAL Input
12	GND	Ground	Ground
13	VCCREG1	VCC Supply	3.3V Supply Voltage for Regulator
14	CP	Analog	Charge Pump
15	REGCAP2	Analog	Regulator Output for External Capacitor
16	VCCREG2	VCC Supply	3.3V Supply Voltage for Regulator

Table 3: Pin Description

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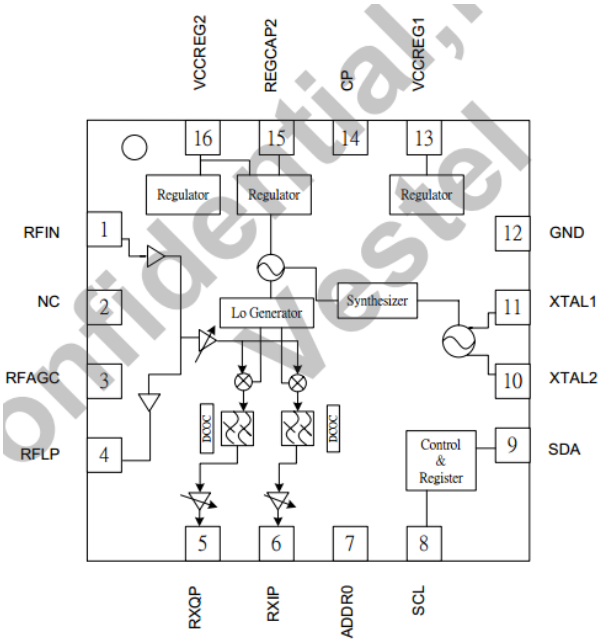


Figure 4: Functional Block Diagram

ITEM	MIN.	MAX.
Power supply voltage (VCCREG1/2)	– 0.3V	4.0V
Pin voltage	– 0.3V	HOST_IO_VCC + 0.3V
Maximum power dissipation	-	0.5W
Operating temperature	– 20°C	+85°C
Storage temperature	– 65°C	+150°C
LNA input level	-	+10dBm
Digital pin	-	+5mA
RFAGC pin	-	+5mA

Table4: Absolute Maximum Ratings

4. AUDIO AMPLIFIER STAGES

A. MAIN AMPLIFIER (U62)(6-8-10 W OPTİON)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I^2C digital control interface, the user can control AD82587D's input format selection, mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)

    - 32kHz / 44.1kHz / 48kHz and
    - 64kHz / 88.2kHz / 96kHz and
    - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
    - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz
    - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
    - 64x~256x Fs for 128kHz /176.4kHz/192kHz
- Supply voltage
    - 3.3V for digital circuit
    - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
    - 10W x 2ch into 8_ @ 0.16% THD+N
    - 15W x 2ch into 8_ @ 0.18% THD+N
    - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
    - 20W x 1ch into 4_ @ 0.17% THD+N
    - 30W x 1ch into 4_ @ 0.2% THD+N
    - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
    - Volume control (+24dB~-103dB, 0.125dB/step)
    - Dynamic range control
    - Power clipping
    - Channel mixing
    - User programmed noise gate with hysteresis window
    - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

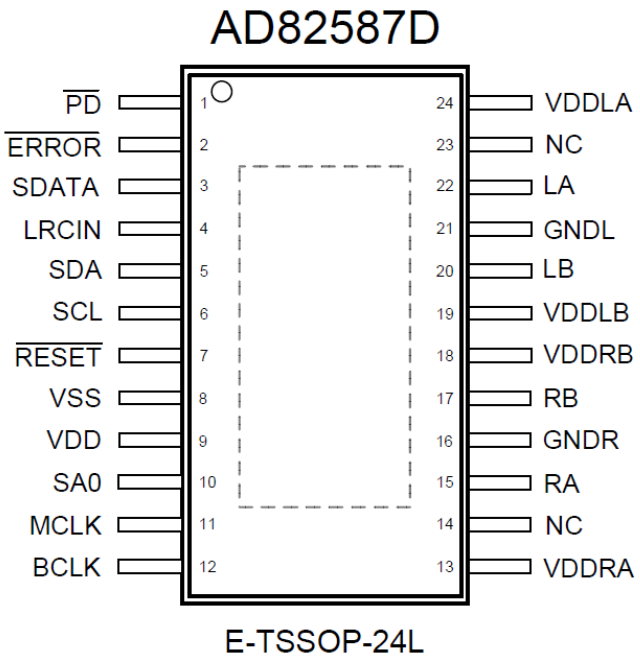


Figure: Pin description

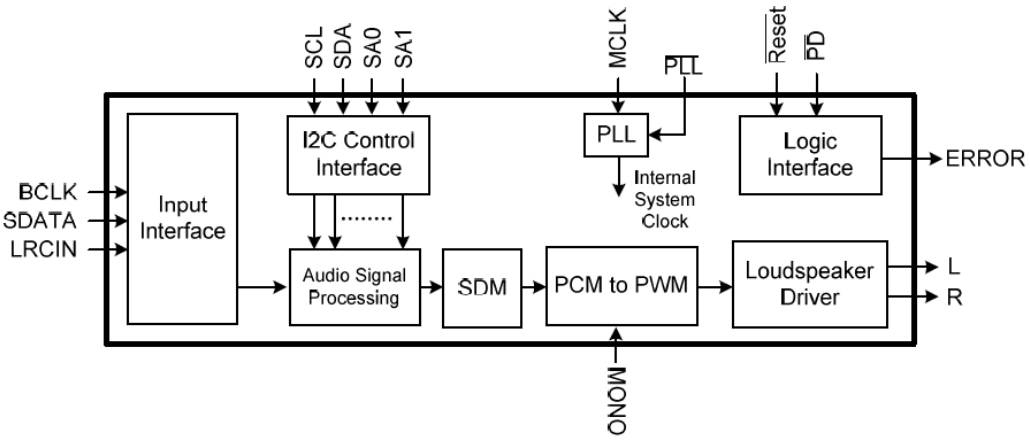


Figure: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table: Recommended Operating Conditions

B. MAIN AMPLIFIER (U91)(2.5 W OPTION)

Description

The AD52010 is a 3.0W stereo, filter-less class-D audio amplifier. Operating with 5.0V loudspeaker driver supply, it can deliver 3.0W output power into 4 ohm loudspeaker within 10% THD+N or 2.6W at 1% THD+N. The AD52010 is a stereo audio amplifier with high efficiency and suitable for the notebook computer, and portable multimedia device.

Features

- Supply voltage range: 2.5 V to 5.5 V
- Support single-ended or differential analog input
- Low Quiescent Current
- Low Output Noise
- Low shut-down current
- Short power-on transient time
- Internal pull-low resistor on shut-down pins
- Short-circuit protection
- Over-temperature protection
- Loudspeaker power within 10% THD+N
    - 1.78W/ch into 8 ohm loudspeaker
    - >3W/ch into 4 ohm loudspeaker
- Loudspeaker efficiency
    - 93% @ 8 ohm, THD+N=10%
    - 85% @ 4 ohm, THD+N=10%
- E-TSSOP-14L package
- Integrated Feedback Resistor of 300kW

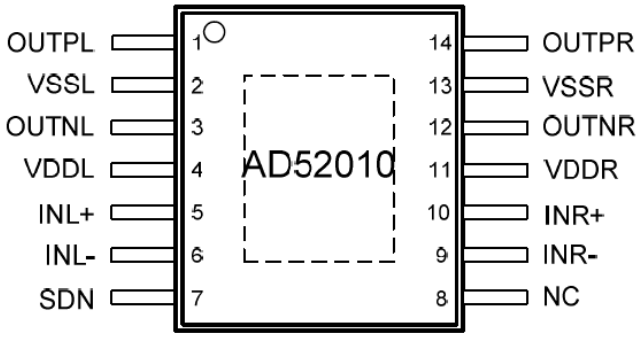


Figure: Pin description

NAME	PIN	IO TYPE	DESCRIPTION
	E-TSSOP-14		
OUTPL	1	O	Positive output for left channel.
VSSL	2	G	Power ground for left channel.
OUTNL	3	O	Negative output for left channel.
VDDL	4	P	Power supply for left channel.
INL+	5	I	Positive differential input for left channel.
INL-	6	I	Negative differential input for left channel.
SDN	7	I	Shutdown AD52010 (Low active logic).
NC	8	NC	No internal connected.
INR-	9	I	Negative differential input for right channel.
INR+	10	I	Positive differential input for right channel.
VDDR	11	P	Power supply for right channel.
OUTNR	12	O	Negative output for right channel.
VSSR	13	G	Power ground for right channel.
OUTPR	14	O	Positive output for right channel.
Thermal pad	N/A	G	To connect the package exposed pad to PCB for thermal power dissipation.

Table:Pin functions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply for analog cells & loudspeaker driver	2.5	5.5	V
V_{IH}	High-Level Input Voltage	1.3	-	V
V_{IL}	Low-Level Input Voltage	-	0.35	V
T_J	Junction operating temperature	-40	125	℃
Ta	Ambient Operating Temperature	-40	85	℃

Table: Recommended operating conditions

C. HEADPHONE AMPLIFIER (U85)

Description

The AD22657B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22657B is capable of delivering 2-Vrms output into a 10k ohm load with 3.3V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22657B has under voltage protection to prevent POP noise. Build-in shutdown control and de-pop control sequence also help AD22657B to be a pop-less device.

The AD22657B is available in a 10-pin MSOP package.

Features

- Operation Voltage: 3V to 3.6V
- Cap-less Output
  - Eliminates Output Capacitors
  - Improves Low Frequency Response
  - Reduces POP/Clicks

- Low Noise and THD
  - Typical SNR 107dB
  - Typical Vn 7uVrms
  - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
  - 2Vrms at 3.3V Supply Voltage
- Single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time: 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection
- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

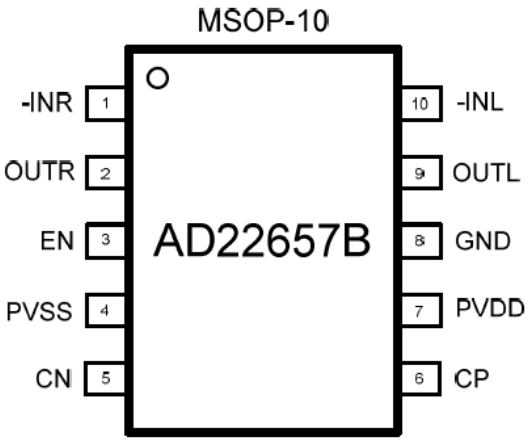


Figure: Pin description

No.	Name	Type (1)	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

Table: Pin functions

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	℃
R_L	Load Resistance		600			Ω

Table: Recommended operating conditions

5. POWER STAGE

Power socket is used for taking voltages which are 12V_stby and 24V (VDD_Audio for 10W option via power_pin1). These voltages are produced in power card. Also socket is used for giving dimming, backlight and stand-by signals with power card. It is shown in figure.

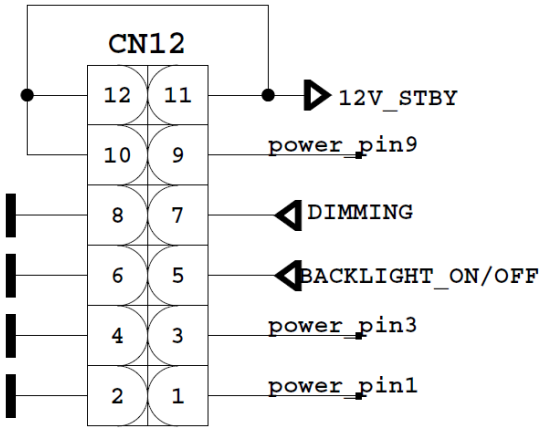
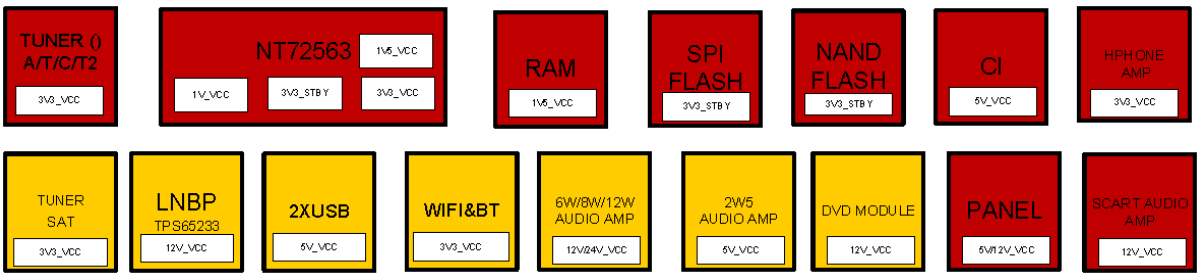
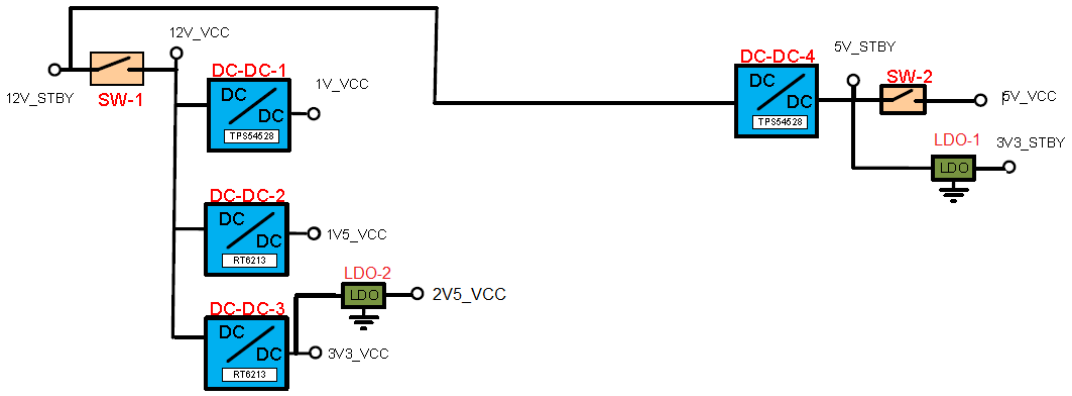


Figure: Power socket and power options





List of the components are:

- SW1(Q61) → FDC642P
- SW2(Q77) → DMG6402LDM
- DC-DC1(U2) → TPS54528
- DC-DC2 (U128) → TPS562201
- DC-DC3 (U129) → RT6213BHGJ6F
- DC-DC4 (U63) → RT7278G (12V panel option)
- DC-DC4 (U63) → TPS54528 (5V panel option)
- LDO1(U131) → AP2111H
- LDO2(U143) → APL5910

A. FDC642P

Description and Features

Single P-Channel 2.5V Specified PowerTrench® MOSFET

-20 V, -4.0 A, 65 mΩ

Features

- Max $r_{DS(on)}$ = 65 mΩ at V_{GS} = -4.5 V, I_D = -4.0 A
- Max $r_{DS(on)}$ = 100 mΩ at V_{GS} = -2.5 V, I_D = -3.2 A
- Fast switching speed
- Low gate charge (11nC typical)
- High performance trench technology for extremely low $r_{DS(on)}$
- SuperSOT™-6 package: small footprint (72% smaller than standard SO-8); low profile (1 mm thick)
- Termination is Lead-free and RoHS Compliant

General Description

This P-Channel 2.5V specified MOSFET is produced using Fairchild's advanced PowerTrench® process that has been especially tailored to minimize on-state resistance and yet maintain low gate charge for superior switching performance.

These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the larger packages are impractical.

Applications

- Load switch
- Battery protection
- Power management

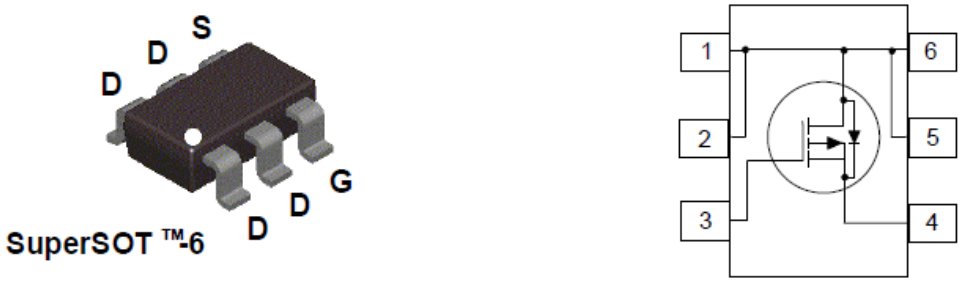


Figure: Pin description

B. DMG6402LDM

Features

- Low RDS(ON)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage
- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

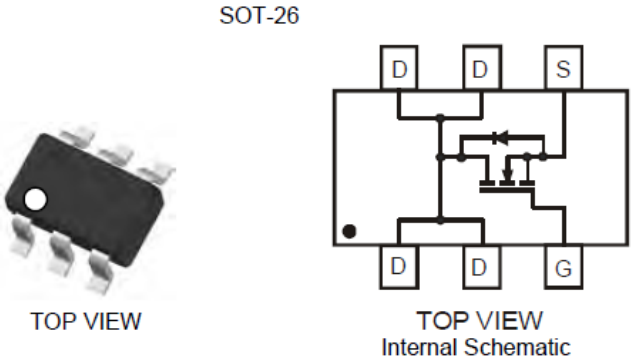


Figure: Pin description

C. TPS54528

Description

The TPS54528 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6.0 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-pin DDA package, and designed to operate from –40 C to 85 C.

Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6.0 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
    - 65 mΩ (High Side) and 36 mΩ (Low Side)
- High Efficiency, less than 10 µA at shutdown

- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (fSW)
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode™ for High Efficiency at Light Load

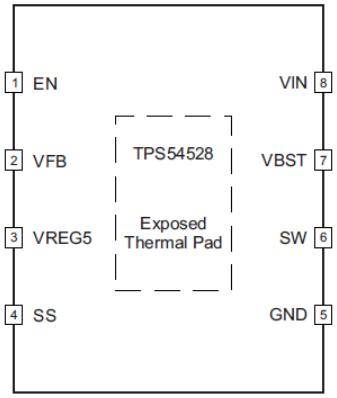


Figure: Pin description

PIN		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply pin.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table: Pin functions

D. TPS562201

Description

The TPS562201 is simple, easy-touse, 2-A synchronous step-down converter in SOT- 23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current. These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components. The TPS562201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS562201 and TPS562208 are available in a 6- pin 1.6 × 2.9 (mm) SOT (DDC) package and specified from –40°C to 125°C of junction temperature.

Features

- TPS562201 and TPS562208 2-A Converter Integrated 140-mΩ and 84-mΩ FETs
- D-CAP2™ Mode Control With Fast Transient Response

- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Pulse-Skip Mode (TPS562201) or Continuous Current Mode (TPS562208)
- 580-kHz Switching Frequency
- Low Shutdown Current Less than 10 µA
- 2% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-by-Cycle Overcurrent Limit
- Hiccup-Mode Overcurrent Protection
- Non-Latch UVP and TSD Protections
- Fixed Soft-Start: 1.0 ms

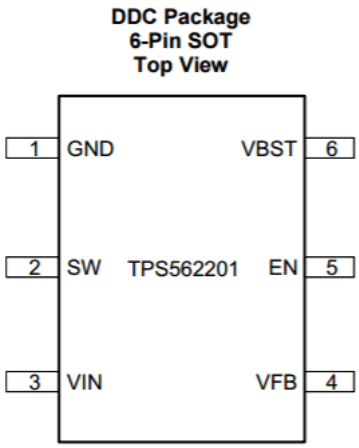


Figure: Pin description

Pin Functions

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect 0.1-µF capacitor between VBST and SW pins.

E. RT7278

Description

The RT7278 is a synchronous step down converter with Advanced Constant On-Time (ACOTTM) mode control. The ACOTTM provides a very fast transient response with few external components. The low impedance internal MOSFET supports high efficiency operation with wide input voltage range from 4.5V to 17V. The proprietary circuit of the RT7278 enables to support all ceramic capacitors. The output voltage can be adjustable between 0.8V and 8V. The soft-start is adjustable by an external capacitor.

Features

- ACOT^{TM} Mode Enables Fast Transient Response
- 4.5V to 17V Input Voltage Range
- 3A Output Current
- 60mΩ Internal Low Site N-MOSFET
- Advanced Constant On-Time Control
- Support All Ceramic Capacitors
- Up to 95% Efficiency
- 700kHz Switching Frequency
- Adjustable Output Voltage from 0.8V to 8V
- Adjustable Soft-Start
- Cycle-by-Cycle Current Limit
- Input Under Voltage Lockout
- Thermal Shutdown Protection
- RoHS Compliant and Halogen Free

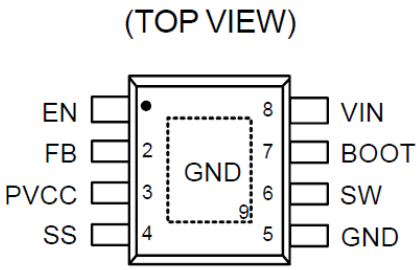


Figure: Pin description

Pin No.		Pin Name	Pin Function
SOP-8 (Exposed Pad)	WDFN-10L 3x3		
1	1	EN	Enable Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	2	FB	Feedback Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback reference voltage is 0.765V typically.
3	3	PVCC	Internal Regulator Output. Connect a 1μF capacitor to GND to stabilize output voltage.
4	4	SS	Soft-Start Control Input. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 1.5ms.
5, 9 (Exposed Pad)	5, 11 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	6, 7	SW	Switch Node. Connect this pin to an external L-C filter.
7	8	BOOT	Bootstrap for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	9, 10	VIN	Supply Input. The input voltage range is from 4.5V to 17V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Table: Pin functions

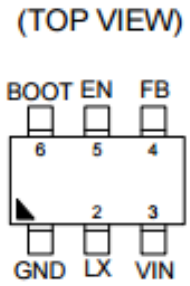
F. RT6213

Description

The RT6213A/B is a high-efficiency, monolithic synchronous step-down DC/DC converter that can deliver up to 3A peak output current from a 4.5V to 18V input supply. The RT6213A/B adopts ACOT architecture to allow the transient response to be improved and keep in constant frequency. Cycle-by-cycle current limit provides protection against shorted outputs and soft-start eliminates input current surge during start-up. Fault conditions also include output under voltage protection, output over current protection, and thermal shutdown.

Features

- Integrated 150mΩ/70mΩ MOSFETs
- 4.5V to 18V Supply Voltage Range
- 500kHz Switching Frequency
- ACOT Control
- 0.8V ± 1.5% Voltage Reference
- Internal Start-Up into Pre-biased Outputs
- Compact Package: TSOT-23-6 pin
- Input Under-Voltage Lockout
- Over-Current Protection and Hiccup



TSOT-23-6 (FC)

Figure: Pin description

Pin No.	Pin Name	Pin Function
1	GND	System Ground. Provides the ground return path for the control circuitry and low-side power MOSFET.
2	LX	Switch Node. LX is the switching node that supplies power to the output and connect the output LC filter from LX to the output load.
3	VIN	Power Input. Supplies the power switches of the device.
4	FB	Feedback Voltage Input. This pin is used to set the desired output voltage via an external resistive divider. The feedback voltage is 0.8V typically.
5	EN	Enable Control Input. Floating this pin or connecting this pin to GND can disable the device and connecting this pin to logic high can enable the device.
6	BOOT	Bootstrap Supply for High-Side Gate Driver. Connect a 100nF or greater capacitor from LX to BOOT to power the high-side switch.

Table: Pin functions

G. LM1117

Description

The LM1117 is a series of low dropout voltage regulators with a dropout of 1.2V at 800mA of load current. It has the same pin-out as National Semiconductor's industry Standard LM317.

The LM1117 is available in an adjustable version, which can set the output voltage from 1.25V to 13.8V with only two external resistors. In addition, it is also available in five fixed voltages, 1.8V, 2.5V, 2.85V, 3.3V, and 5V.

The LM1117 offers current limiting and thermal shutdown. Its circuit includes a zener trimmed bandgap reference to assure output voltage accuracy to within ±1%.

The LM1117 series is available in SOT-223, TO-220, and TO-252 D-PAK packages. A minimum of 10µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8V, 2.5V, 2.85V, 3.3V, 5V, and Adjustable Versions
- Space Saving SOT-223 Package
- Current Limiting and Thermal Protection
- Output Current 800mA
- Line Regulation 0.2% (Max)
- Load Regulation 0.4% (Max)
- Temperature Range

— LM1117 0°C to 125°C

— LM1117I −40°C to 125°C

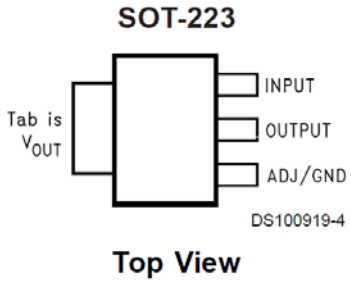


Figure: Pin description

H. APL5910

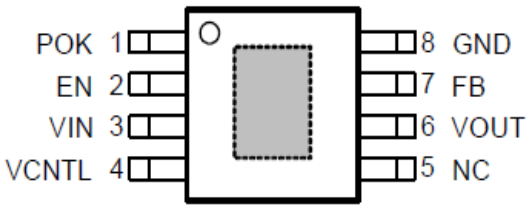
Description

The APL5910 is a 1A ultra low dropout linear regulator. The IC needs two supply voltages, one is a control voltage (VCNTL) for the control circuitry, the other is a main supply voltage (VIN) for power conversion, to reduce power dissipation and provide extremely low dropout voltage. The APL5910 integrates many functions. A Power-On- Reset (POR) circuit monitors both supply voltages on VCNTL and VIN pins to prevent erroneous operations. The functions of thermal shutdown and current-limit protect the device against thermal and current over-loads. A POK indicates that the output voltage status with a delay time set internally. It can control other converter for power sequence. The APL5910 can be enabled by other power systems. Pulling and holding the EN voltage below 0.4V shuts off the output.

The APL5910 is available in a SOP-8P package which features small size as SOP-8 and an Exposed Pad to reduce the junction-to-case resistance to extend power range of applications.

Features

- Ultra Low Dropout
  - 0.12V (Typical) at 1AOutput Current
- 0.8V Reference Voltage
- High Output Accuracy
  - ±1.5%over Line, Load, and Temperature Range
- Fast Transient Response
- Adjustable Output Voltage
- Power-On-Reset Monitoring on Both VCNTL and VIN Pins
- Internal Soft-Start
- Current-Limit and ShortCurrent-Limit Protections
- Thermal Shutdown with Hysteresis
- Open-Drain VOUT Voltage Indicator (POK)
- Low Shutdown Quiescent Current (< 30mA)
- Shutdown/Enable Control Function
- Simple SOP-8P Package with Exposed Pad
- Lead Free and Green Devices Available (RoHS Compliant)



SOP-8P (Top View)

Figure: Pin description

PIN		FUNCTION
NO.	NAME	
1	POK	Power-OK signal output pin. This pin is an open-drain output used to indicate the status of output voltage by sensing FB voltage. This pin is pulled low when output voltage is not within the Power-OK voltage window.
2	EN	Active-high enable control pin. Applying and holding the voltage on this pin below the enable voltage threshold shuts down the output. When re-enabled, the IC undergoes a new soft-start process. When left this pin open, an internal pull-up current (5μA typical) pulls the EN voltage and enables the regulator.
3	VIN	Main supply input pin for voltage conversions. A decoupling capacitor (≥10μF recommended) is usually connected near this pin to filter the voltage noise and improve transient response. The voltage on this pin is monitored for Power-On-Reset purpose
4	VCNTL	Bias voltage input pin for internal control circuitry. Connect this pin to a voltage source (+5V recommended). A decoupling capacitor (1μF typical) is usually connected near this pin to filter the voltage noise. The voltage at this pin is monitored for Power-On-Reset purpose.
5	NC	No Connection.
6	VOUT	Output pin of the regulator. Connecting this pin to load and output capacitors (10μF at least) is required for stability and improving transient response. The output voltage is programmed by the resistor-divider connected to FB pin. The VOUT can provide 1A (max.) load current to loads. During shutdown, the output voltage is quickly discharged by an internal pull-low MOSFET.
7	FB	Voltage Feedback Pin. Connecting this pin to an external resistor divider receives the feedback voltage of the regulator.

Table: Pin functions

6. MICROCONTROLLER

NOVATEK NT72563MBG-GA

Description

The NT72563MBGis an integrated digital TV system-on-chip which compliants with variety ATV as NTSC, PAL and SECAM, and DTV standards as ISDB-T, DVB-T/-T2/-C/-S/-S2, ITU-T J.83B, ATSC, integrates DTV and multi-media AV decoder, SIF demodulator, and support A/V post-processing.

The integrated video ADC and video decoder support PC VGA port, YPbPr, BAV-IN, CVBS and S-Video Input. Regarding the tuner input, the digital VIF performs the universal analog TV demodulation (NTSC, PAL, and SECAM), including IF processing, AGC, video demodulation, and second sound IF generation (SSIF).The video decoder supports universal TV video format. The integrated audio ADC supports stereo audio input corresponding to video input sources. The integrated TV sound decoder supports universal TV sound format.

The advanced picture quality and color engine create more vivid image impression than ever. The HDMI receiver v1.4b, supports deep color, CEC features and 3D formats. The USB high speed host supports updating firmware code, multi-media playback from the external USB flash devices.

The standby controller can operate sololy from the main system, powered by the standby power source from power module, consumes as low current as possible. It meets the requirement of Green appliance.

Features

- CPU
  - ARM Cortex A9 Dual
  - Support TrustZone
  - Support PTM
  - Support NEON

- DRAM Interface
  - Internal DDR3 1.6GHz 16-bits 2Gb
  - External DDR3 1.6GHz 16-bits up to 4Gb
  - Spread Spectrum PLL for EMI reduction

- Flash controller
  - NAND type flash
    - RS/BCH Support
  - eMMC 5.1 with HS400 type flash (without support command queue)
  - SPI NOR type flash x1

- Stand-by Controller
  - Support VGA / IR / KeyPad / CEC/ wake-up
  - Built-in Turbo 8051 for stand-by application usage
  - Built-in Low Voltage Reset for brown out
  - Built-in EDID for saving system BOM cost
  - System power control

- Condition Access
  - Support Common Interface
  - Support Common Interface Plus
  - Built-in Cryptograph Engine for conditional access and CI Plus
  - Meet Common Interface Plus's Robust and Compliance rule

- Copy Protection Engine
  - Support Cryptograph Key Protection
  - Support Demux Key Protection
  - Support HDCP Key Protection

- Internal High-Speed Video ADC
  - Integrated triple high speed ADCs/ PLL to support both YPbPr and RGB format signal
  - 10-bits data resolution
  - Maximum conversion up to 165 MSPS
  - Support 0.7 ~ 1.0 Volts analog RGB/YUV input
  - 3:1 analog input MUX
  - Supports both non-interlaced and interlaced input signals

- Analog Video Decoder
  - Clamp and AGC (Automatic Gain Control) circuit to support 0.5 to 1.6V analog input signal
  - Support multi-standards, macro-vision detection and related status report
  - Embedded Teletext Level 2.5 / Close Caption and other VBI Decoder
  - 2D and 3D adaptive Comb Filter for better Y/C Separation
  - Support VPS signal decode for EU channel sorting purpose

- TV encoder with built-in video DAC
  - Built-in 10-bit DAC for CVBS Analog Video output.
  - Support HD resolution input with high quality scaling down engine
  - Support TTX/ CC/ WSS/ VPS/ CGMS-A/ Macrovision insertion

- Digital Video CODEC
  - Built-in multi-standard video codec
  - Support pixel format YUV420 only for all video codec except JPEG
  - H.264 Constrained Baseline/Main/High Profiles @ 1080p60 (Level 4.0 and Level 4.1 under limited bit-rate)
  - VP8 Profiles @ 1080p30
  - VP9 Profile 0, 2 up to 10-bit @ 1080p60
  - AVS(Optional) Jizhun Profile @ 1080p30 (Level 6.0)
  - AVS+(Optional) @ 1080p30
  - VC-1(Optional) Simple/Main/Advanced Profiles @ 1080p30 (Level 3.0)
  - RealVideo(Optional) 8/9/10 @ 1080p30
  - MPEG-4 Simple/Advanced Simple Profiles @ 1080p30
  - H.263 Profile 0 @ 1080p30
  - DivX1 3/4/5/6(Optional) @ 1080p30
  - Sorenson Spark @ 1080p30
  - MPEG-2 Main Profile @ 1080p30
  - MPEG-1 @ 1080p30
  - JPEG baseline sequential mode
    - Support pixel formats in YUV420, YUV422 and YUV444

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- Support Motion JPEG @ 1080p30
- HEVC(H.265) Main 10 profile @1080p60(level 4.1)
- H.264 encoder @ 1080p30, @720p60, @480p60
- JPEG encoder baseline YUV420 @ 1080p10

- De-Interlacing
  - Support progressive scan 24Hz to 85Hz Frame Rate Conversion
  - 5th generation High performance Motion-Adaptive De-interlacing
  - 5th generation Diagonal Edge Enhancement for smoothing edge outline
  - Automatic Video Source Detection
  - Support Inverse 3:2/2:2 pull down and multiple cadence for film stream
  - Scene Change Detection
  - Built-in Anti-Crosscolor to remove abnormal color performance
  - Built-in Color Performance stabilizer for SECAM video format
  - Built-in Region Classifier engine to get flicker free image quality

- Visual Effect Processor
  - Built-in Advanced Super Resolution
  - 5th generation Advanced Scaling Up Engine
  - Support Nonlinear Scaling
  - 5th generation LTI/CTI function
  - Support 5th Color Engine
  - Global Brightness, Contrast, Hue Saturation and Intensity Adjustment
  - Built-in I-Gamma and Black Stretch for Automatic Contrast Adjustment
  - Support sRGB and xvYCC Adjustment Standard
  - De-blocking, De-Mosquito, Temporal and Spatial Noise Filter
  - Adaptively determine 3D noise filter for different noise level
  - Linear Gamut Remapping
  - SD2HD detection and Processing
  - DP Meter for Dynamic backlight Control
  - Support HDR
  - Support Cinema Contrast Enhancer

- Display Processor
  - Embedded dual 10 bit LVDS transmitter
  - Supports single pixel / dual pixel output
  - Dithering function supports 30-bit quality for 24 bit or 18-bit panel
  - Optional Frame Sync or Free Run display synchronization modes
  - Display Resolution up to 1920X1080@60Hz HDTV format
  - Built-in Gamma Correction for different type display device
  - Supports Pivot (H flipping display)
  - V flipping is in LBM
  - Support H/V sync out
  - Video alpha blending

- 3D-Graphic Engine
  - Mali 400 Dual Core
  - Support the MMU function
  - Supports OpenGLES1.x & 2.0,
  - Supports OpenVG 1.0 & 1.1

- 2D-Graphic Engine
  - Bitmap Operation
  - ARGB/RGBA format
  - Copy/Color expansion
  - Logic Operation
  - Copy with alpha blending (only 16/32 bit color mode)
  - Source and destination area could be overlapped
  - Color key for the transparence effect
  - 12 Raster Operation (ROP) rules
  - Fill Rectangle
  - Color fill
  - Gradient fill
  - Scaling
  - Bicubic Algorithm

- OSD
  - 8/16/32-bit OSD Architecture
  - 3 OSD Layers
  - 5 levels of transparency with pixel or frame based operation (background, video, Plane3, Plane2, Plane1, cursor1, cursor2)
  - Support OSD scaling down function
  - Programmable width & height to meet LCD/TV's resolution exactly
  - H/V scaling

- HDMI receiver
  - 3 HDMI Input ports(Port A is HDMI & MHL combo port)
  - Support HDMI PIP
  - HDMI Rx 1.4b Compliant
  - Integrated HDCP 1.4 & 2.2 cipher engine

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for Content Protection
- Support High-Level CEC Command for Easy Link between CE equipments.
- Support Deep Color for more pixel depth information
- Support xvYCC for wide color gamut application
- 3D support
- Support Audio format including
  - 2~8 channels, 32-192KHz
- Support ARC (Audio Return Channel)
- Support Multi-VSIF
- 4K2K 30p HDMI input with scaling down

■ MHL receiver
- CBUS
  - DDC packet
  - MSC(MHL Sideband Channel) packet
  - Vendor-specific packet
  - Packed Pixel mode

■ 3D support
- 2D-to-3D real time conversion
- Support mandatory HDMI 1.4a 3D video format and timing
  - 3D FP
  - 3D SBS
  - 3D TB
- Support 100/120Hz shutter glasses half FHD 3D TV panel
- Line interleave for directly drive 60Hz PR 3D LCD
- Intermediate formats output support external 3D processor
- Support separate and programmable L/R sync pin
- Support Shutter glasses control signals
  - L/R sync signal phase, polarity, duration programmable

■ SIF Demodulator
- NICAM-BG/DK/I/L, A2-BG/DK/I, BTSC, A2-M, AM SECAM-L
- Automatic standard and mode detection
- Automatic carrier mute and automatic NICAM fall back
- 32KHz audio output

■ Audio CODEC (Audio ADC/DAC)
- Built-in 3:1 audio ADC input mux (MAX. sampling rate 48 KHz)
- Built-in 2 audio DAC output (MAX. sampling rate 48 KHz)
- Built-in 3 I2S Output format for Power-Stage Amplifier
- Built-in 1 I2S Input
- S/PDIF output supported

■ Audio Processor
- Dedicated DSP to decode compressed audio
- Supports digital audio format decoding:
  - MPEG-1/2 (Layer I/ II/ III), Dolby Digital (AC3) (Optional), Dolby Digital Plus (EAC3) (Optional), AAC-LC (Optional), HE-AAC (Optional), WMA3 (Optional), WMA (Optional), DTS (Optional)
- Supports Dolby Digital Plus (Optional) and MS10/11 (Optional) multistream decoder, including Dolby Digital Encoder for transcoding streams to Dolby Digital 5.1
- Supports DTS Neo 2:5 (Optional) to transcoding streams to DTS 5.1
- Advance sound processing: Automatic Volume Control, 5-band EQ, Automatic Gain Control, Virtual Surround, Dynamic range control (DRC)
- Advance sound processing options available, for example: DTS Tursurround HD (Optional), DTS Studio Sound (Optional)

■ Digital VIF Demodulator
- Compliant with NTSC, PAL, SECAM video standards for universal analog terrestrial and cable support
- Support for FM-A2(IRT-A2), AM, BTSC+SAP, EIA-J, MK-A2, NICAM audio standards
- Support Low IF, 5 ~ 8 MHz (silicon tuner)
- Single IF AGC control with ΔΣ modulation
- Flexible channel bandwidth (6 MHz, 7 MHz, and 8 MHz)
- Digital video and audio dual-path split processor

■ ISDB-T Demodulator
- Compliant with ISDB-T standard ARIB STD-B31 and SBTVD standard ABNT NBR 15601
- Receiver specifications ARIB STD-B21 & ABNT NBR 15604 fulfilled
- Channel bandwidth 6, 7 & 8 MHz

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supported
- Low IF with configurable mixing frequency
- Single IF AGC controls with ΔΣ modulation
- Partial (1-segment) & full (13-segment) reception supported
- Non-hierarchical (single-layer) & hierarchical (layers A/B/C) reception supported
- Automatic detection of transmission parameters:
  - Modes 1 (2k), 2 (4k), 3 (8k)
  - Guard intervals of 1/4, 1/8, 1/16, 1/32
  - Constellations DQPSK, QPSK, 16QAM, 64QAM
  - Code rates of 1/2, 2/3, 3/4, 5/6, 7/8
- Start flag for emergency-alarm broadcasting
- Robust TMCC decoding
- Impulsive noise reduction
- Adjacent-channel interference suppression
- Superior AWGN & SFN performance
- Superior co-channel interference performance
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±400 kHz (6 MHz bandwidth)
- Performance monitoring: SNR (dB), pre-Viterbi BER, post-Viterbi BER, RS uncorrectable error count

■ DVB-T Demodulator
- Compliant with ETSI EN 300 744, NorDig Unified 2.5.1, D-Book 7 Part A v3, and Digitenne 4.0.4 fulfilled
- Channel bandwidth 6, 7 & 8 MHz supported
- Low-IF with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Non-hierarchical & hierarchical (high-priority / low-priority) reception supported
- Automatic detection of transmission parameters:
  - 2K/8K modes
  - Guard intervals of 1/4, 1/8, 1/16, 1/32
  - Constellations QPSK, 16QAM, 64QAM
  - Code rates of 1/2, 2/3, 3/4, 5/6, 7/8
- Robust TPS decoding
- Impulsive noise reduction
- Adjacent channel interference (ACI) filter and Co-channel interference (CCI) suppression
- Superior AWGN & SFN performance
- Timing acquisition range: ±100 ppm
- Carrier acquisition range: ±650 kHz (8 MHz bandwidth)
- Performance monitoring: SNR (dB), pre-Viterbi BER, post-Viterbi BER, RS uncorrectable error count

■ DVB-C Demodulator
- Compliant with ETSI EN 300 429 DVB-C Receiver specifications NorDig Unified 2.2.2, Ziggo and China HD_GY/T 241-2009 fulfilled
- Low-IF with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Variable Symbol Rates supported: 1 MBaud ~ 7.2 MBaud
- Constellation supported: 16/32/64/128/256- QAM
- Matched Filters (Roll-off factor= 0.15)
- Robust blind adaptive equalizer
- Superior impulsive noise cancellation
- High monitoring capabilities
  - C/N ratio (SNR)
  - Signal Power
  - RS uncorrectable error Number

■ ATSC Demodulator
- ATSC A.53d compatible
- Low IF supported with configurable mixing frequency
- Single IF AGC control with ΔΣ modulation
- Carrier recovery with or without pilot
- Excellent ATSC 50-channel reception performance
- Excellent phase noise tracking performance
- Pass Brazil A/B/C/D/E

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- Excellent CCI rejection performance
- Timing acquisition range: ±200 ppm
- Carrier acquisition range: ±200 kHz
- Performance monitoring: SNR, BER, RS uncorrectable error count

- J.83B Demodulator
  - ITU J.83B compatible
  - Low IF supported with configurable mixing frequency
  - Single IF AGC control with ΔΣ modulation
  - 64/256QAM automatic detection
  - Excellent phase noise tracking performance
  - Excellent co-channel single tone rejection capability
  - Timing acquisition range: ±800 ppm
  - Carrier acquisition range: ±400 kHz (64QAM)
  - Robust blind adaptive equalizer
  - Superior impulsive noise cancellation
  - Performance monitoring: SNR, BER, RS uncorrectable error count

- DVB-T2
  - DVB-T2 standard ETSI EN 302 755 compliant
  - NorDig-Unified 2.5.1 and D-Book 7 Part A v3 requirements fulfilled
  - Channel BW 1.7, 5, 6, 7, 8 MHz
  - All single-profile DVB-T2 modes supported, including
    - T2-Base profile
    - T2-Lite profile
    - Single and Multiple PLPs
    - SISO and MISO transmissions
    - Rotated and non-rotated constellations
    - Scrambled L1-post signaling
    - PAPR
    - FEF skipped automatically
  - Low-IF supported with configurable mixing frequency
  - Carrier acquisition range: ±650 kHz @ 8 MHz BW
  - Timing acquisition range: ±100 ppm
  - Automatic spectral inversion detection
  - Superior Single Frequency Network performance
  - Excellent co-channel interference suppression
  - Fast channel zapping

- DVB-S/S2
  - Compliant to ETSI EN 300 421 DVB-S and EN 302 307 DVB-S2 Broadcast Services
  - QPSK, 8PSK, 16APSK and 32APSK
  - QPSK/8PSK 1 ~ 45Msps, 16APSK: 1 ~ 39Msps and 32APSK 1 ~ 32Msps
  - Blind Scan
  - Differential and single end IQ input
  - Dual ADC interface
  - IQ mismatch removal
  - Automatic spectrum inversion
  - DiSEqCTM v2.2

- Ethernet
  - Built-in 10/100 Ethernet MAC and PHY
  - Support WOL

- USB host/device controller with built in transceiver
  - 4 USB host ports
  - Compliant with USB Specification Revision 2.0
  - Support high-speed, full-speed and low-speed devices
  - Integrated USB 2.0 transceiver

- LED backlight
  - PWM x 2
  - PWM delay and duty is adjustable individually
  - PWM delay is phase-locked to VS
  - Support PWM frequency = 1 x VS , 2 x VS frequency
  - SPI LED-driver interface

- Miscellaneous
  - Built-in UART controller
  - HS-LFBGA 19 x 19 (424 Balls)

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Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	0.95V power supply	0.9215	0.97	1.0185	V
$V_{1.5V}$	1.5V power supply (DDR3)	1.425	1.5	1.575	V
$V_{1.8V}$	1.8V power supply (eMMC)	1.7	1.8	1.9	V
$V_{2.5V}$	2.5V power supply	2.375	2.5	2.625	V
V_{DDIO}	3.3V power supply	3.135	3.3	3.465	V
V_{IN3}	3.3V I/O with 5V Tolerance	0	3.3	5.25	V
	Input voltage of 3.3V I/O	0	3.3	3.465	V

Table: Recommended operating conditions

7. 4GB DDR3 SDRAM

HYNİX H5TQ4G63EFR-TEC 2133 (U72)

Description

The H5TQ4G83EFR-xxC,H5TQ4G63EFR-xxC, H5TQ4G83EFR-xxI, H5TQ4G63EFR-xxI, H5TQ4G83EFR-xxL, H5TQ4G63EFR-xxL, H5TQ4G83EFR-xxJ and H5TQ4G63EFR-xxJ are a 4,294,967,296-bit CMOS Double Data Rate III (DDR3) Synchronous DRAM, ideally suited for the main memory applications which requires large memory density and high bandwidth. SK Hynix 4Gb DDR3 SDRAMs offer fully synchronous operations referenced to both rising and falling edges of the clock. While all addresses and control inputs are latched on the rising edges of the CK (falling edges of the CK), Data, Data strobes and Write data masks inputs are sampled on both rising and falling edges of it. The data paths are internally pipelined and 8-bit prefetched to achieve very high bandwidth.

Features

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK, CK) operation
- Differential Data Strobe (DQS, DQS)
- On chip DLL align DQ, DQS and DQS transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8, 9 and 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase of 0 oC~ 95 oC)
- 7.8 μs at 0oC ~ 85 oC
- 3.9 μs at 85oC ~ 95 oC
- Commercial Temperature(0oC ~ 95 oC)
- Industrial Temperature(-40oC ~ 95 oC)
- JEDEC standard 78ball FBGA(x8), 96ball FBGA (x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported

- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
VDD	Supply Voltage	1.425	1.500	1.575	V	1,2
VDDQ	Supply Voltage for Output	1.425	1.500	1.575	V	1,2

Table: Recommended operating conditions

8. 4GBİT (256M X 8 BİT) NAND FLASH MEMORY

MT29F4G08ABAEAWP (U133)

Description

Micron NAND Flash devices include an asynchronous data interface for high-performance I/O operations. These devices use a highly multiplexed 8-bit bus (I/Ox) to transfer commands, address, and data. There are five control signals used to implement the asynchronous data interface: CE#, CLE, ALE, WE#, and RE#. Additional signals control hardware write protection and monitor device status (R/B#). This hardware interface creates a low pin-count device with a standard pinout that remains the same from one density to another, enabling future upgrades to higher densities with no board redesign. A target is the unit of memory accessed by a chip enable signal. A target contains one or more NAND Flash die. A NAND Flash die is the minimum unit that can independently execute commands and report status. A NAND Flash die, in the ONFI specification, is referred to as a logical unit (LUN). There is at least one NAND Flash die per chip enable signal. For further details, see Device and Array Organization. This device has an internal 4-bit ECC that can be enabled using the GET/SET features or by factory (always enabled). See Internal ECC and Spare Area Mapping for ECC for more information.

Features

- Open NAND Flash Interface (ONFI) 1.0-compliant
- Single-level cell (SLC) technology
- Organization
  - Page size x8: 4320 bytes (4096 + 224 bytes)
  - Page size x16: 2160 words (2048 + 112 words)
  - Block size: 64 pages (256K + 14K bytes)
  - Plane size: 2 planes x 1024 blocks per plane
  - Device size: 4Gb: 2048 blocks
- Asynchronous I/O performance
  - ^{t}RC/^{t}WC: 20ns (3.3V), 30ns (1.8V)
- Array performance
  - Read page: 25µs
  - Program page: 200µs (TYP)
  - Erase block: 2ms (TYP)

- Command set: ONFI NAND Flash Protocol
- Advanced command set
    - Program page cache mode
    - Read page cache mode
    - One-time programmable (OTP) mode
    - Programmable drive strength
    - Two-plane commands
    - Multi-die (LUN) operations
    - Read unique ID
    - Block lock (1.8V only)
    - Internal data move
- Operation status byte provides software method for detecting
    - Operation completion
    - Pass/fail condition
    - Write-protect status
- Ready/Busy# (R/B#) signal provides a hardware method of detecting operation completion
- WP# signal: Write protect entire device
- First block (block address 00h) is valid when shipped from factory with ECC. For minimum required ECC, see Error Management.
- RESET (FFh) required as first command after power-on
- Alternate method of device initialization after power up (contact factory)
- Internal data move operations supported within the plane from which data is read
- Quality and reliability
    - Data retention: JESD47G-compliant; see qualification report
    - Endurance: See Qualification Report
- Operating voltage range
    - VCC: 2.7–3.6V
    - VCC: 1.7–1.95V
- Operating temperature:
    - Commercial: 0°C to +70°C
    - Industrial (IT): –40ºC to +85ºC

- Package
  - 48-pin TSOP type 1, CPL2
  - 63-ball VFBGA

Parameter/Condition		Symbol	Min	Typ	Max	Unit
Operating temperature	Commercial	T_A	0	–	70	°C
	Industrial		–40	–	85	°C
Vcc supply voltage	1.8V	V_{CC}	1.7	1.8	1.95	V
	3.3V		2.7	3.3	3.6	V
Ground supply voltage		V_{SS}	0	0	0	V

Table: Recommended operating conditions

9. 16M-BIT [16M X 1] CMOS SERIAL FLASH EEPROM

KH25L1606EM2-12G MACRONİX SPI FLASH (U81)

Description

The device features a serial peripheral interface and software protocol allowing operation on a simple 3-wire bus. The three bus signals are a clock input (SCLK), a serial data input (SI), and a serial data output (SO). Serial access to the device is enabled by CS# input. When it is in Dual Output read mode, the SI and SO pins become SIO0 and SIO1 pins for data output. The device provides sequential read operation on whole chip. After program/erase command is issued, auto program/erase algorithms which program/erase and verify the specified page or sector/block locations will be executed. Program command is executed on byte basis, or page basis, or word basis for erase command is executes on sector, or block, or whole chip basis. To provide user with ease of interface, a status register is included to indicate the status of the chip. The status read command can be issued to detect completion status of a program or erase operation via WIP bit. Advanced security features enhance the protection and security functions; please see security features section for more details.

When the device is not in operation and CS# is high, it is put in standby mode. The device utilizes Macronix's proprietary memory cell, which reliably stores memory contents even after typical 100,000 programs and erase cycles.

Features

- Single Power Supply Operation
  - 2.7 to 3.6 volt for read, erase, and program operations
- Serial Peripheral Interface compatible -- Mode 0 and Mode 3
- 16,777,216 x 1 bit structure or 8,388,608 x 2 bits (Dual Output mode) structure
- 512 Equal Sectors with 4K byte each
  - Any Sector can be erased individually
- 32 Equal Blocks with 64K byte each
  - Any Block can be erased individually
- Program Capability
  - Byte base
  - Page base (256 bytes)

- Latch-up protected to 100mA from -1V to Vcc +1V

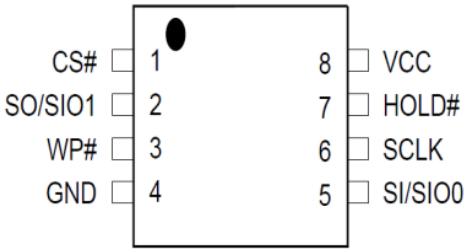


Figure: Pin configuration

SYMBOL	DESCRIPTION
CS#	Chip Select
SI/SIO0	Serial Data Input (for 1 x I/O)/ Serial Data Input & Output (for Dual Output mode)
SO/SIO1	Serial Data Output (for 1 x I/O)/ Serial Data Output (for Dual Output mode)
SCLK	Clock Input
WP#	Write protection
HOLD#	Hold, to pause the device without deselecting the device
VCC	+ 3.3V Power Supply
GND	Ground

Table: Pin description

10. USB INTERFACE

Novatek IC has four input ports for USB, and therefore it doesn't need any hub IC.

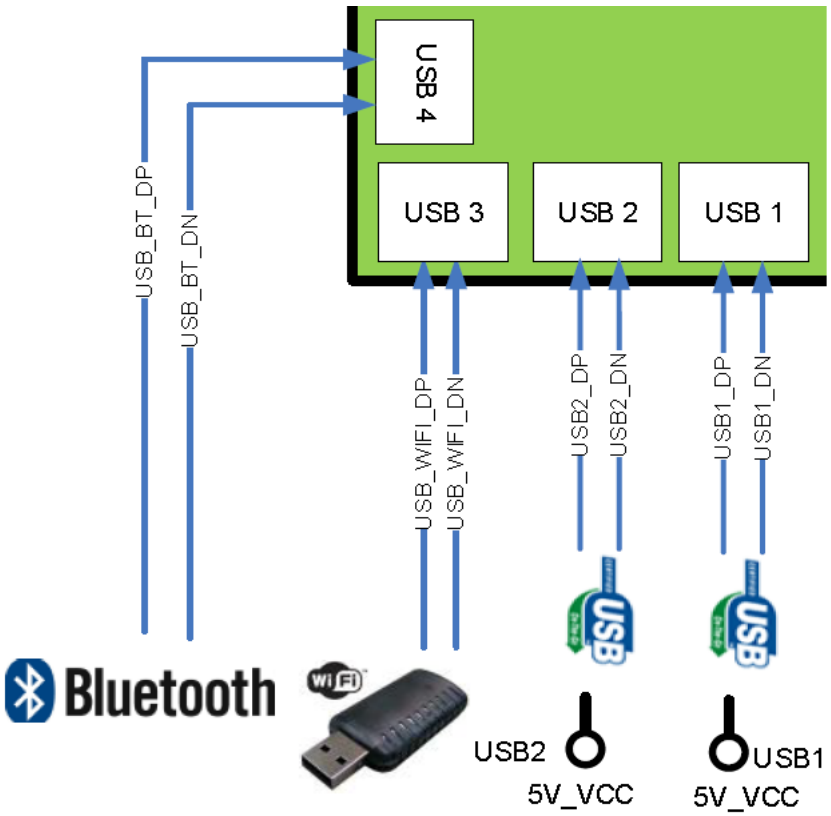


Figure: USB Block Diagram

11. CI INTERFACE

17MB211 Digital CI ve Smart Card Interface Block diagram:

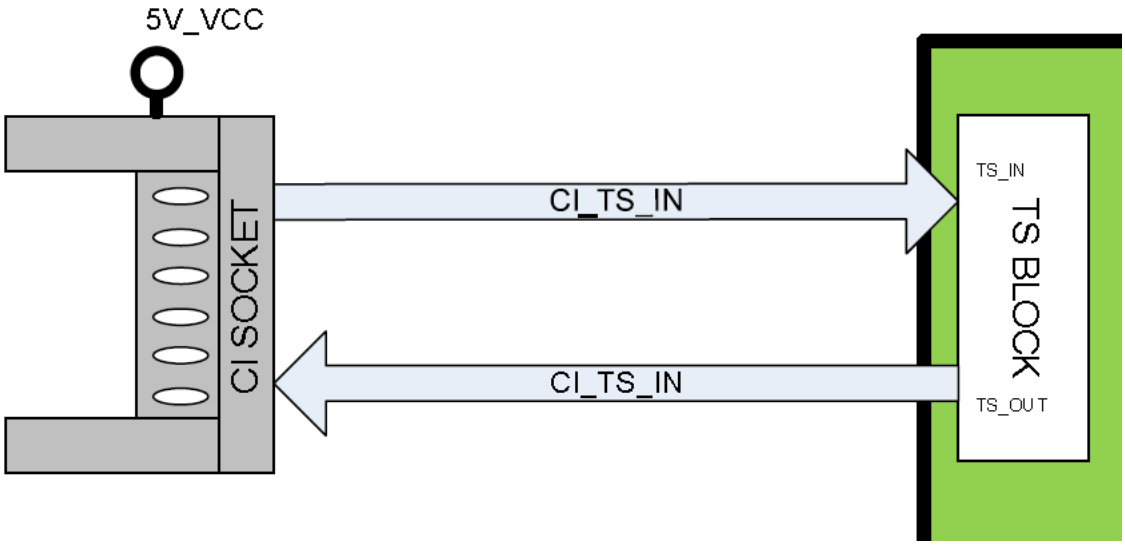


Figure: CI interface

12. SOFTWARE UPDATE

MAIN SW UPDATE

In MB211 project, please follow software update procedure:

1. shredder_usb_update.bin, shredder_usb_update.scr, shredder_usb_update.scr.core and upgrade_mb211.bin files should be copied directly inside of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.
3. While pushing the OK button in remote control, power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

13. TROUBLESHOOTING

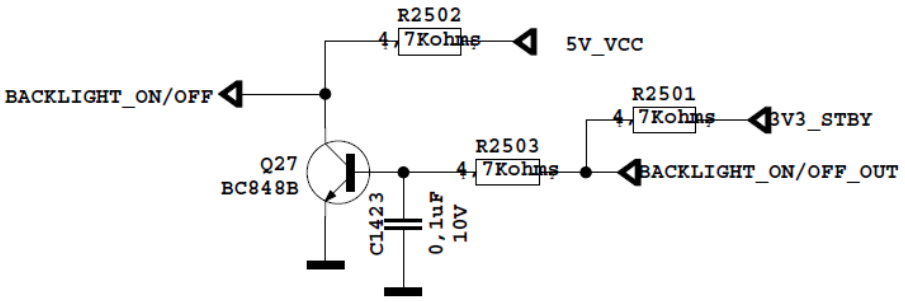
A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

Possible causes: Backlight pin, dimming pin, backlight supply (Panel_VCC), stby on/off pin

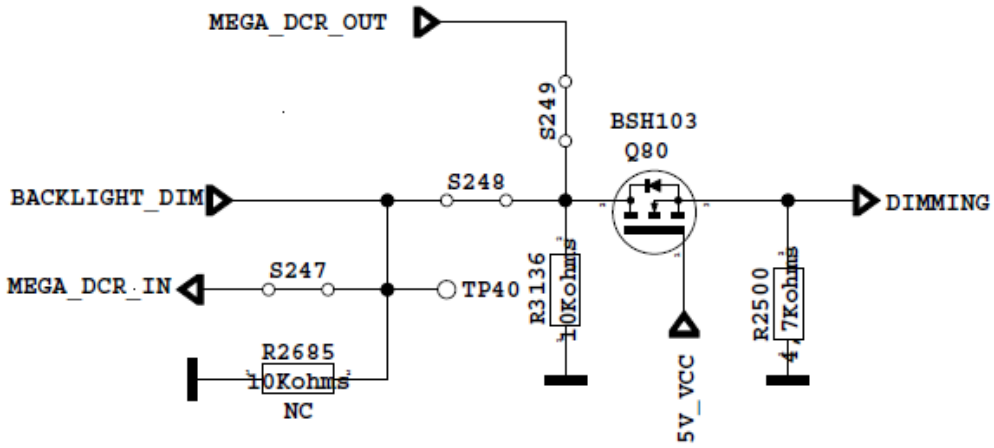
BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q27 must be low when the backlight is OFF. If it is a problem, please check Q27 and the panel cables. Also it can be tested in TP87 in main board.

Backlight On/Off Circuit

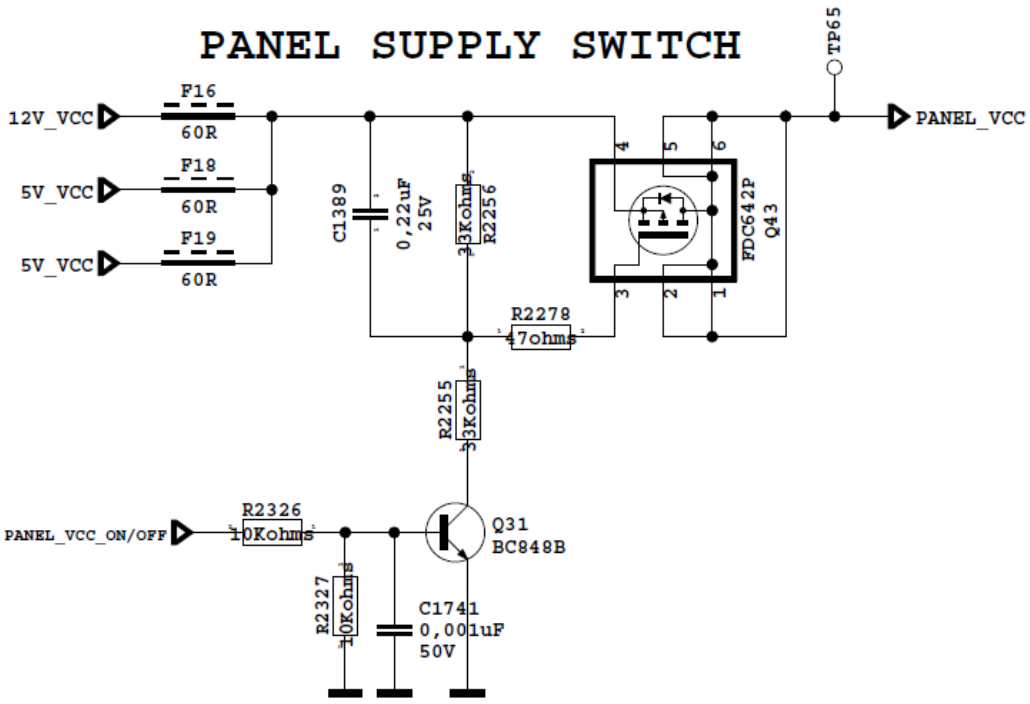


Dimming pin should be high or square wave in open position. If it is low, please check S248 for Novatek side and panel or power cables, connectors.

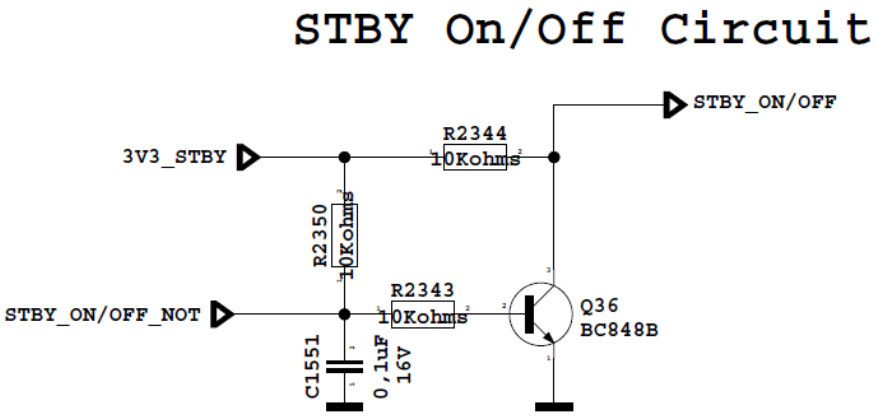
DIMMING



Backlight power supply (Panel_VCC) should be in panel specs. Please check Q43, shown below; also it can be checked TP65.



STBY_ON/OFF should be low for TV on condition, please check Q36's collector.

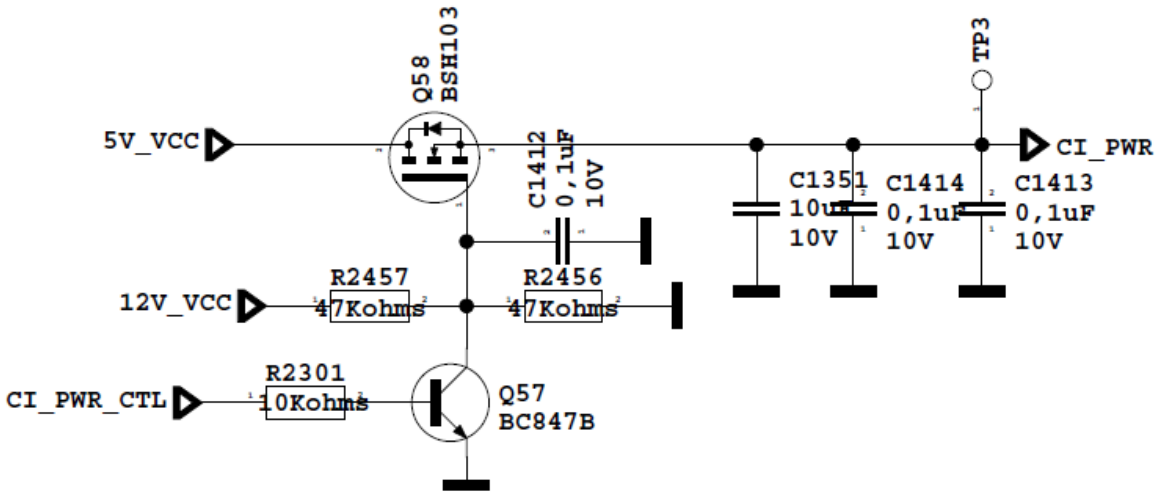


B. CI MODULE PROBLEM

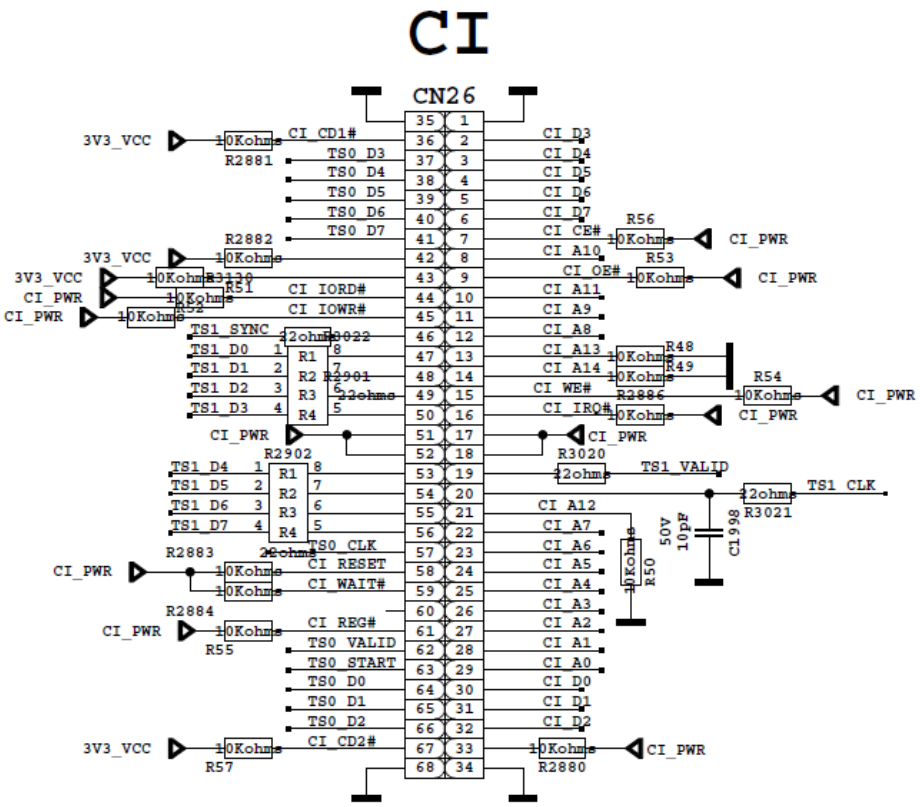
Problem: CI is not working when CI module inserted.

Possible causes: Supply, suply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTL, this pin should be low.



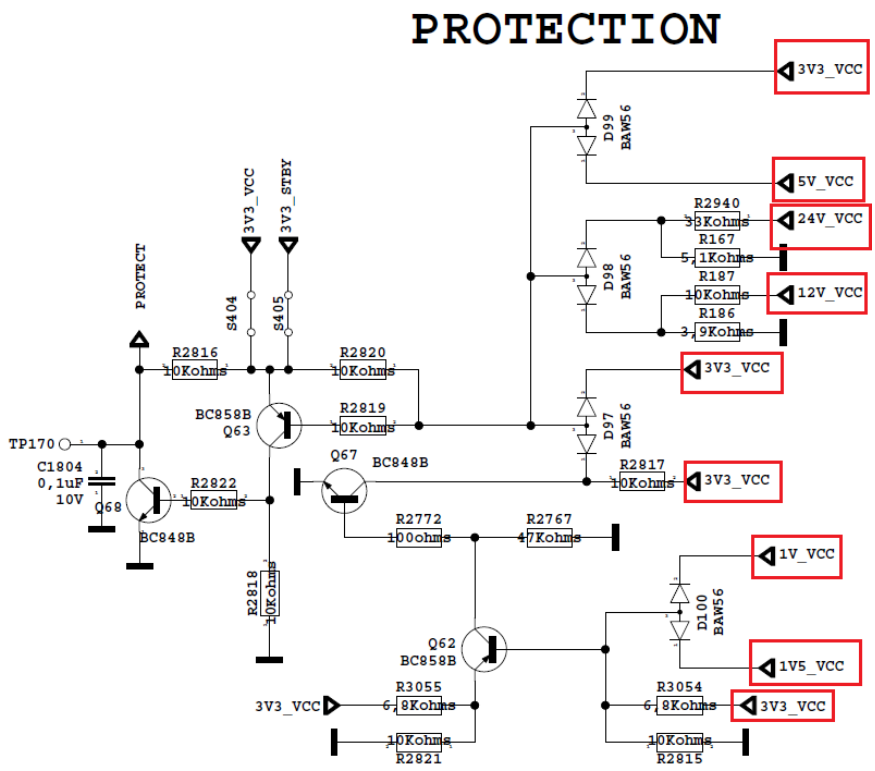
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. STAYING IN STAND-BY MODE

Problem: Staying in stand-by mode, no other operation.

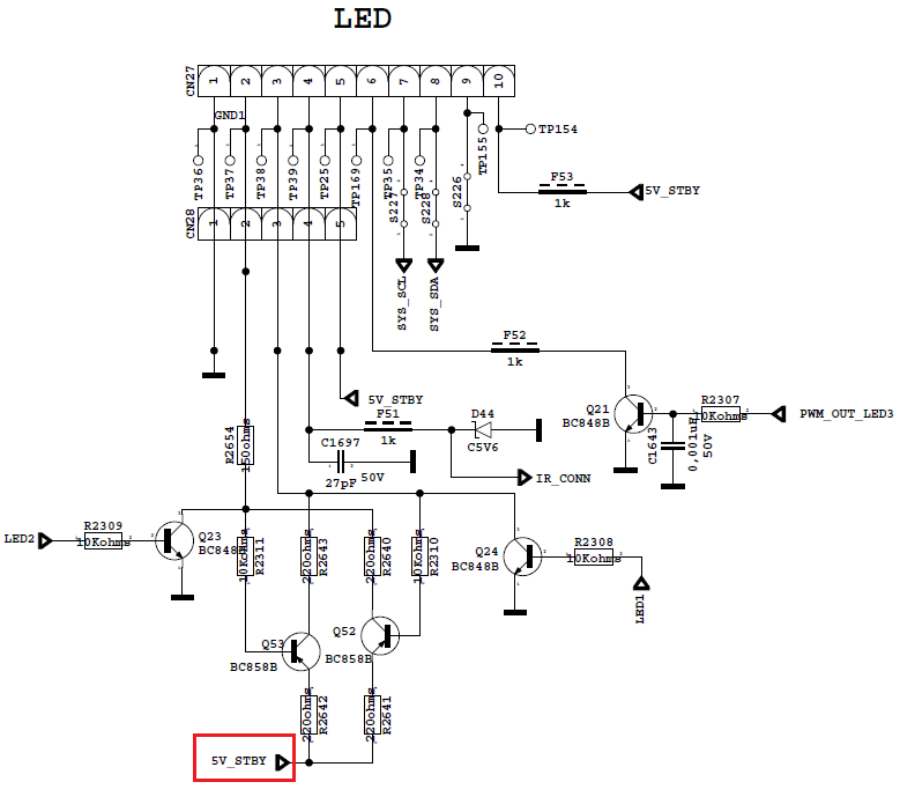
This problem indicates a short on Vcc voltages. Protect pin should be logic high while normal operation. When there is a short circuit protect pin will be logic low. If you detect logic low on protect pin, unplug the TV set and control voltage points with a multimeter to find the shorted voltage to ground.



D. IR PROBLEM

Problem: LED or IR not working

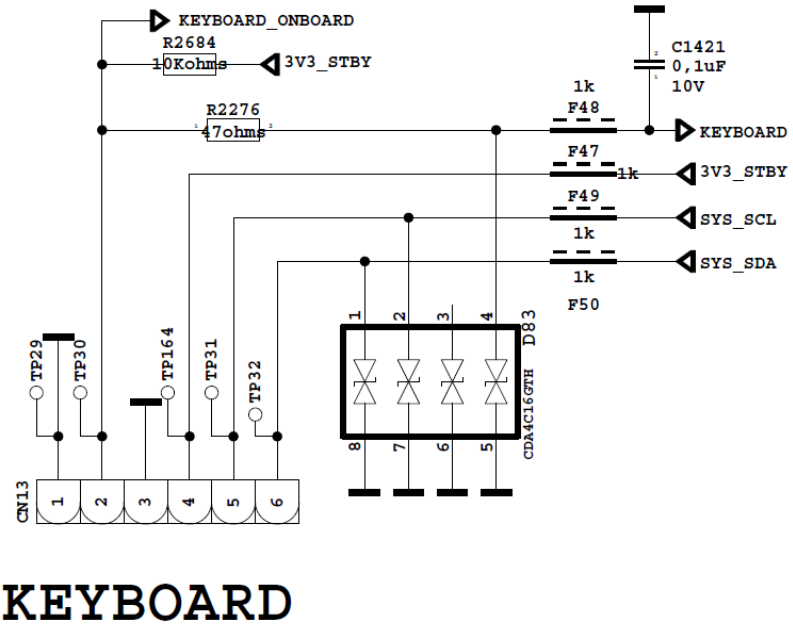
Check LED card supply on MB211 chasis.



E. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

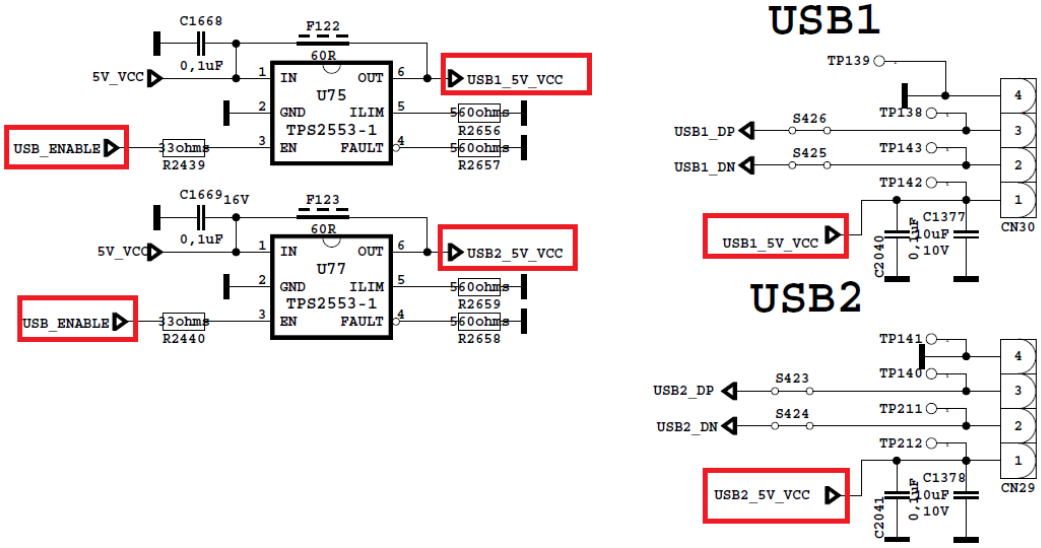
Check keypad supply on MB211.



F. USB PROBLEMS

Problem: USB is not working or no USB Detection.

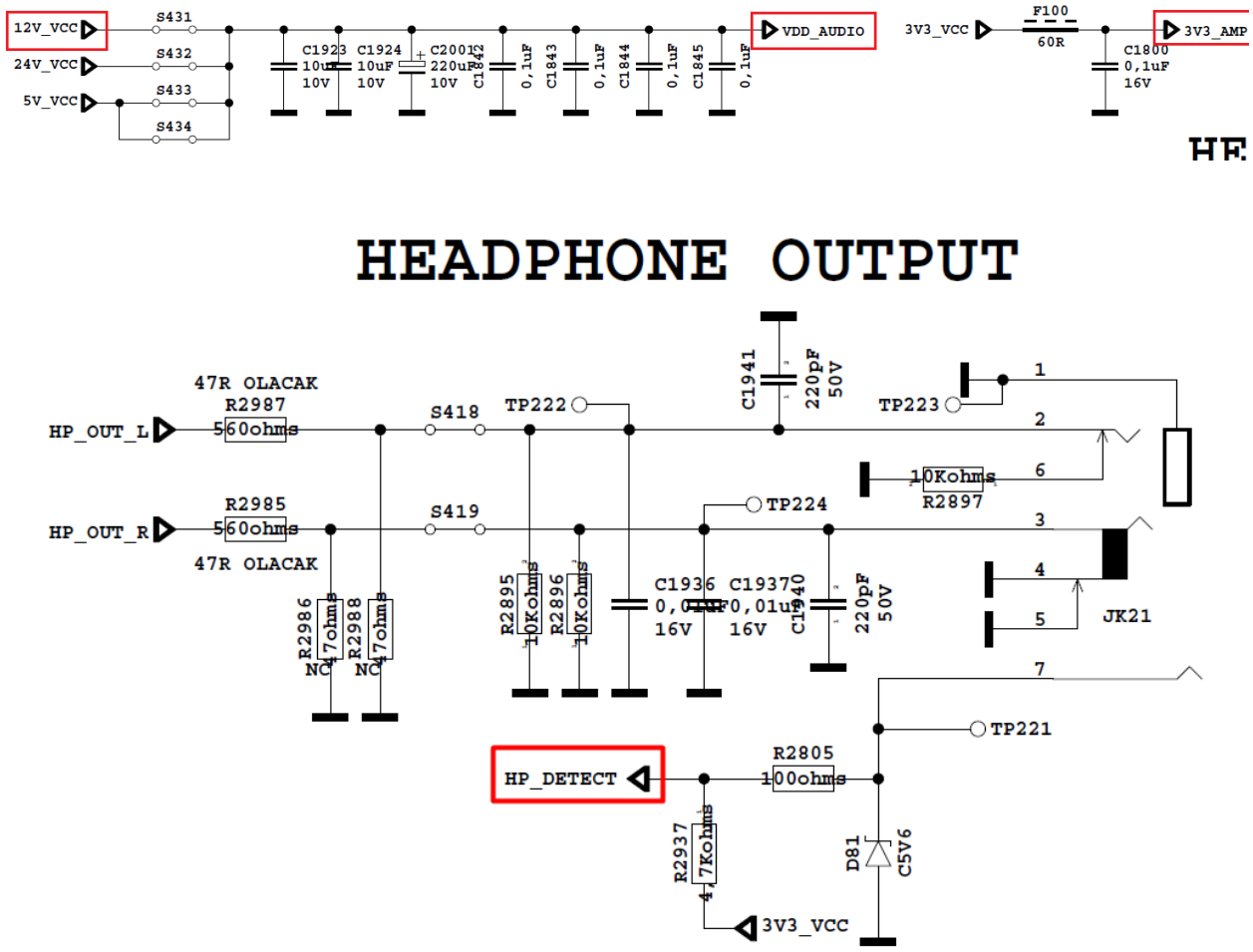
Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.



G. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 12V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit (when headphone is connected, speakers are automatically muted). Measure voltage at HP_DETECT pin, it should be 3.3v.



H. STANDBY ON/OFF PROBLEM

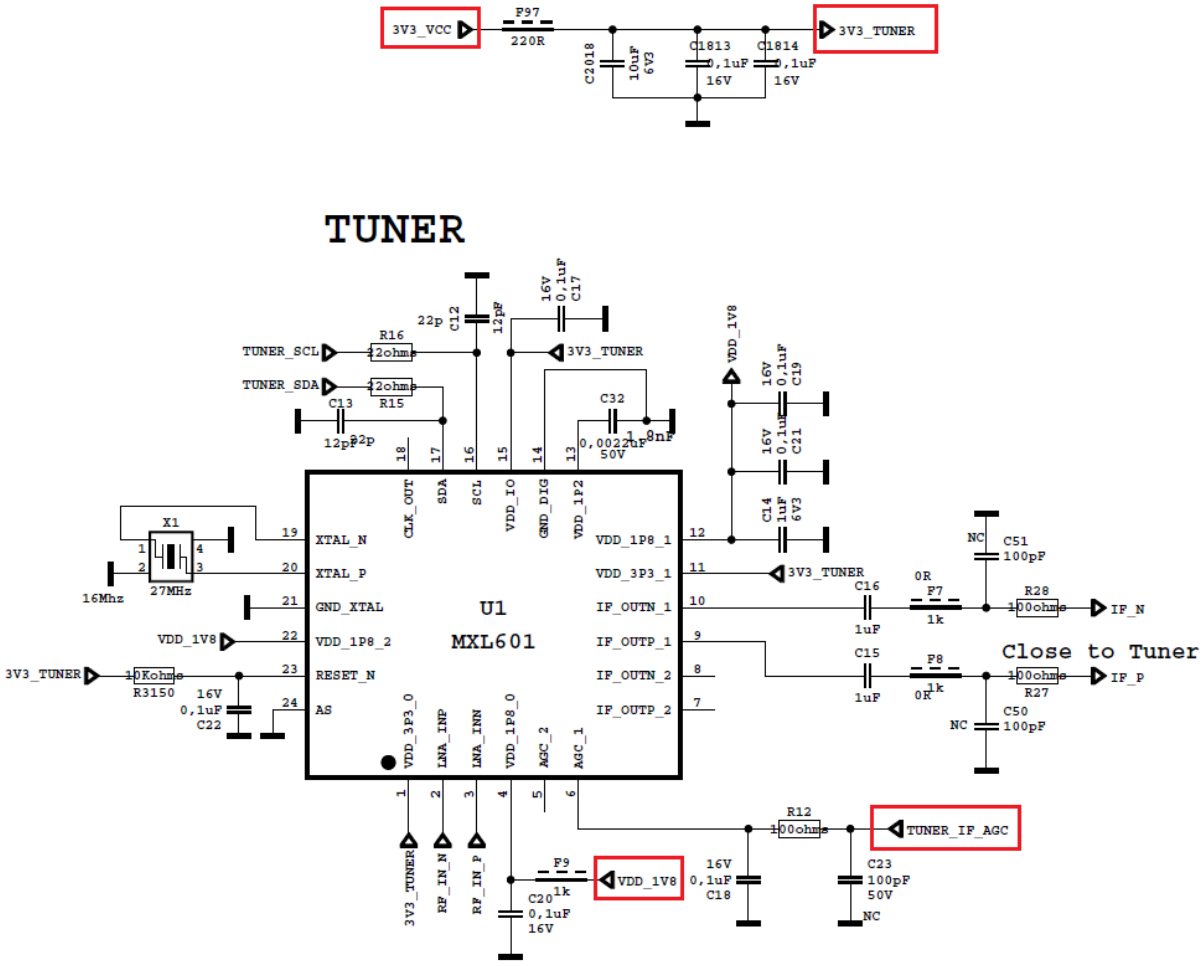
Problem: Device can not boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm. These printouts may give a clue about the problem. You can use VGA for terraterm connection.

I. NO SIGNAL PROBLEM

Problem: No signal in DVB-T/T2/C mode.

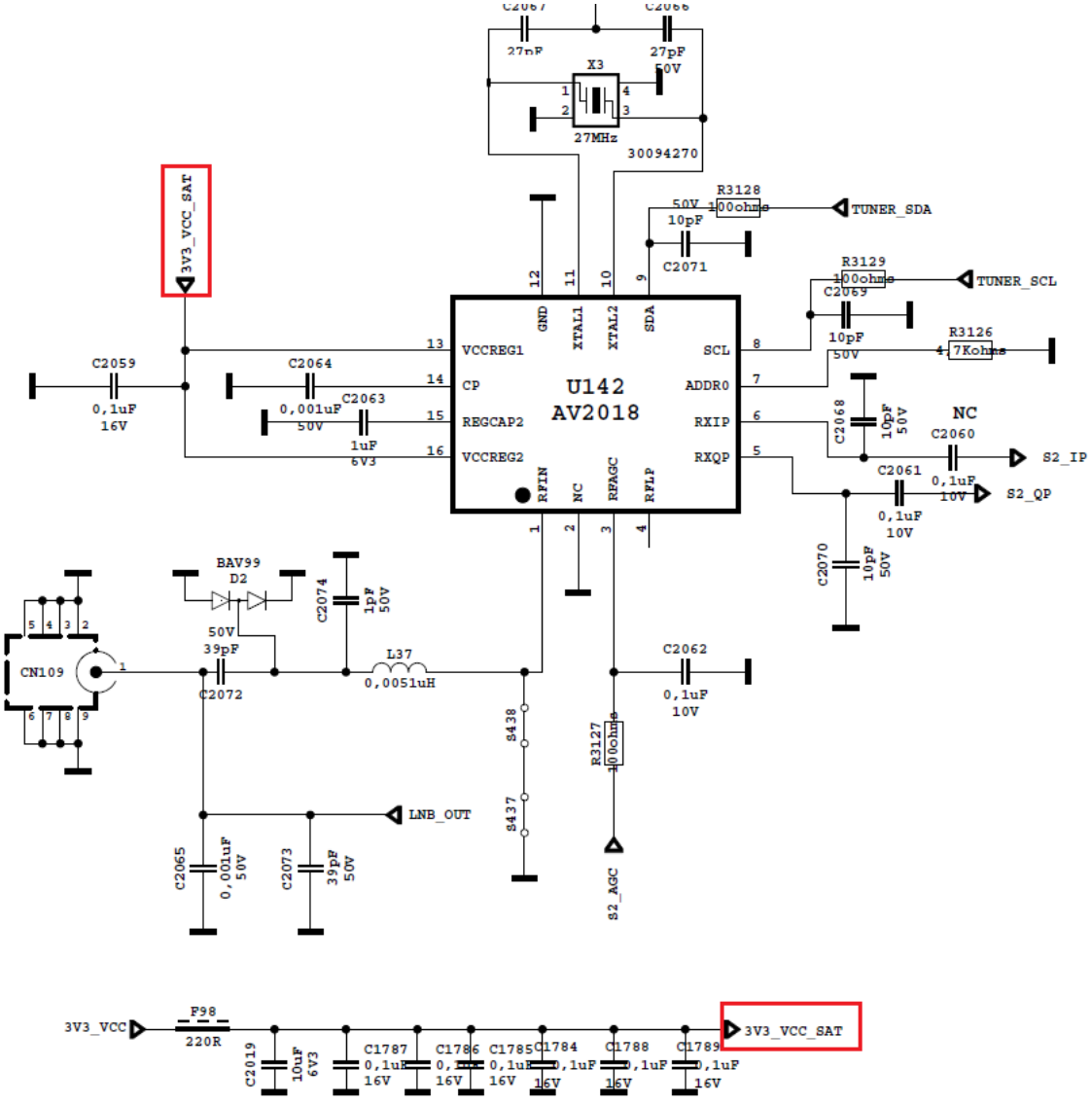
Check tuner supply voltage; 3V3_TUNER and VDD_1V8. Check tuner options are correctly set in Service menu. Check AGC voltage at TUNER_IF_AGC pin of tuner.



Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check AV2018 supply voltage 3V3_VCC_SAT. If it is OK, then measure the voltage from the PIN1 of U142.

If the PIN1 voltage is equal to 0V, please check i2c waveforms and software. If the PIN1 voltage is lower than 1V (e.g: 0.8Vor 0.3V), change the U142 with a new part.

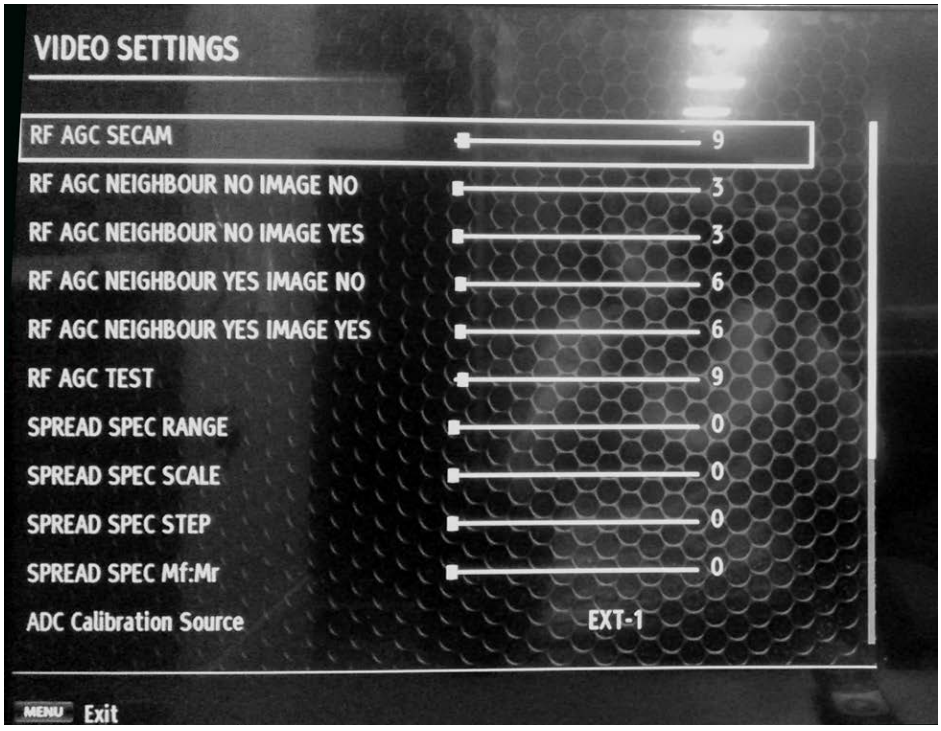

C2067
27nF
C2066
27pF
50V
X3
27MHz
30094270
3V3_VCC_SAT
R3128
50V 100ohms
TUNER_SDA
10pF
C2071
R3129
100ohms
TUNER_SCL
C2069
10pF
50V
R3126
7Kohms
U142
AV2018
GND
XTAL1
XTAL2
SDA
SCL
ADDR0
RXIP
RXQP
VCCREG1
CP
REGCAP2
VCCREG2
RFIN
NC
RFAGC
RFLP
C2059
0,1uF
16V
C2064
0,001uF
50V
C2063
1uF
6V3
C2068
10pF
50V
NC
C2060
S2_IP
C2061
0,1uF
10V
S2_QP
0,1uF
10V
C2070
10pF
50V
BAV99
D2
C2074
1pF
50V
50V
39pF
C2072
L37
0,0051uH
CN109
C2062
0,1uF
10V
R3127
100ohms
S438
S437
LNB_OUT
S2_AGC
C2065
0,001uF
50V
C2073
39pF
50V
3V3_VCC
F98
220R
C2019
10uF
6V3
C1787
0,1uF
16V
C1786
C1785
0,1uF
16V
C1784
0,1uF
16V
C1788
0,1uF
16V
C1789
0,1uF
16V
3V3_VCC_SAT

14. SERVICE MENU SETTINGS

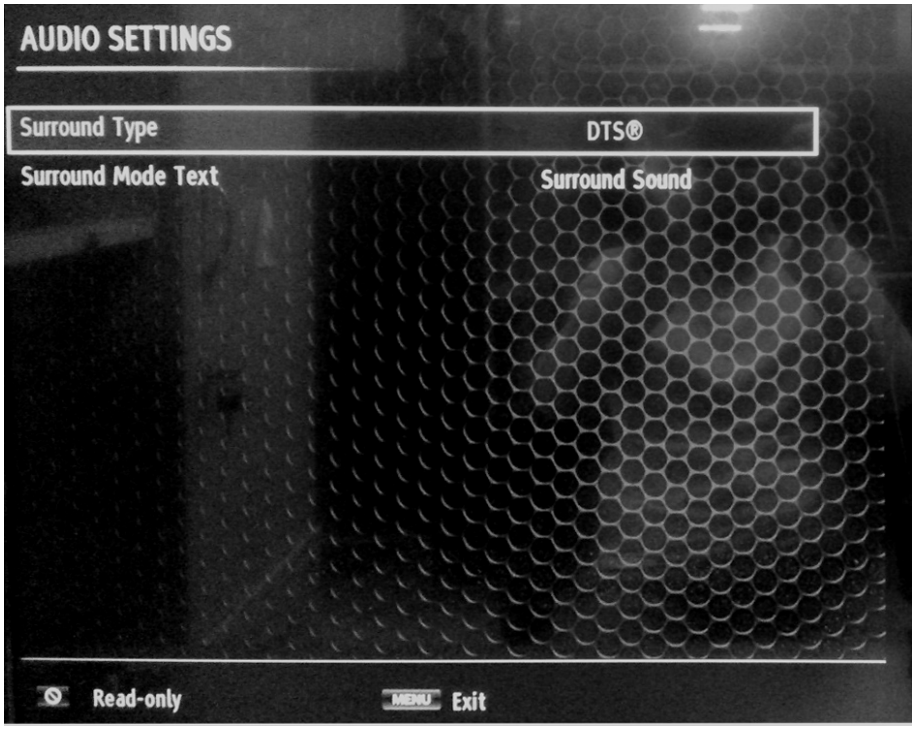
In order to reach service menu, first Press **"MENU"** buton, then write "**4725"** by using remote controller.

You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.

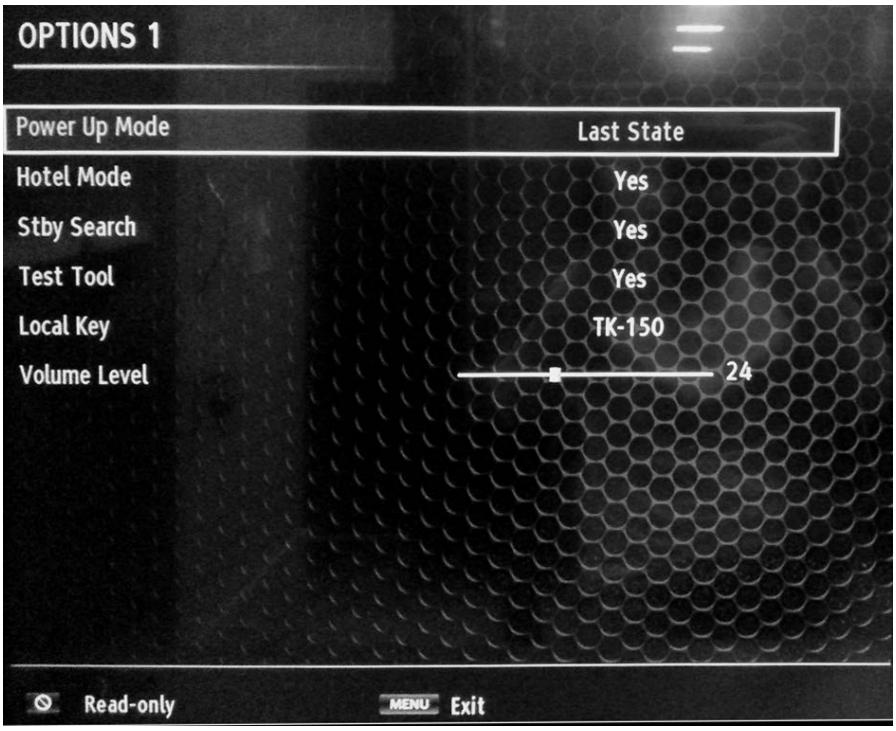
Service Menu Main Screen



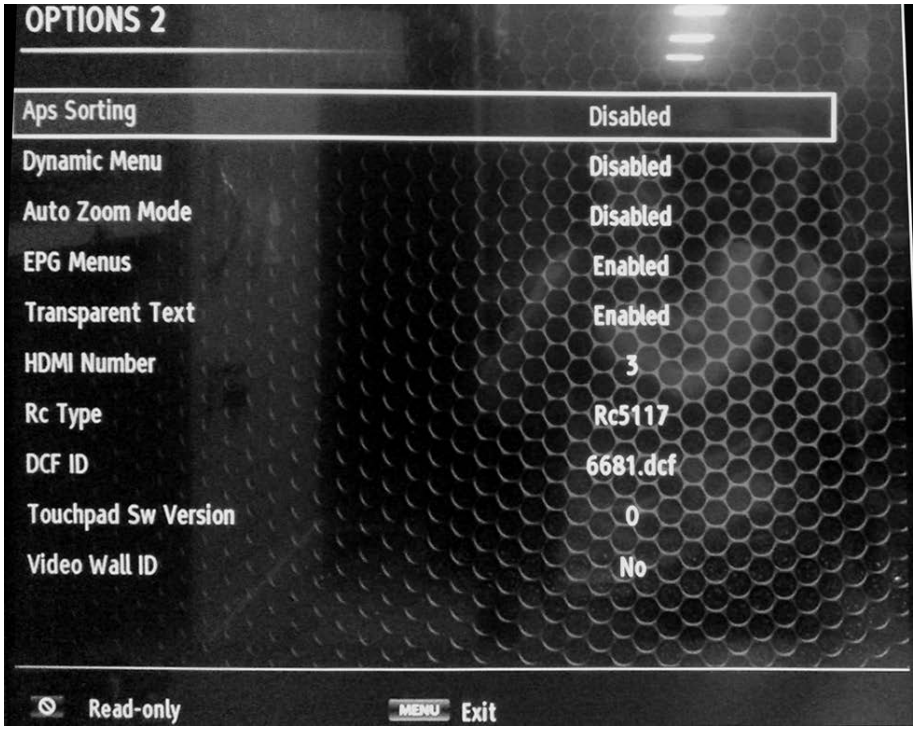
Video Settings



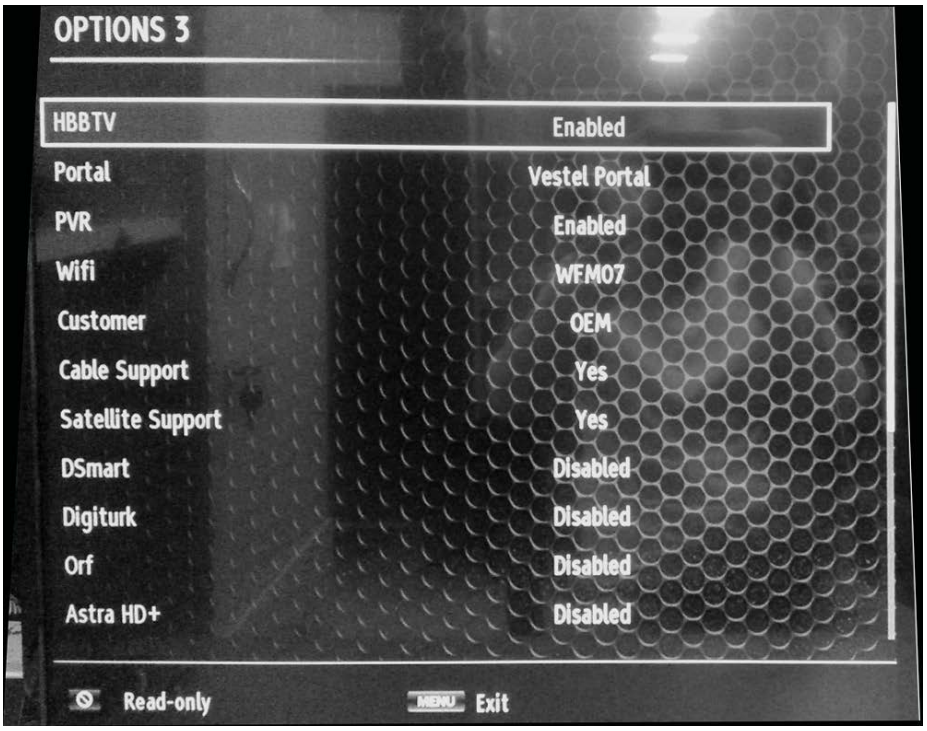
Audio Settings



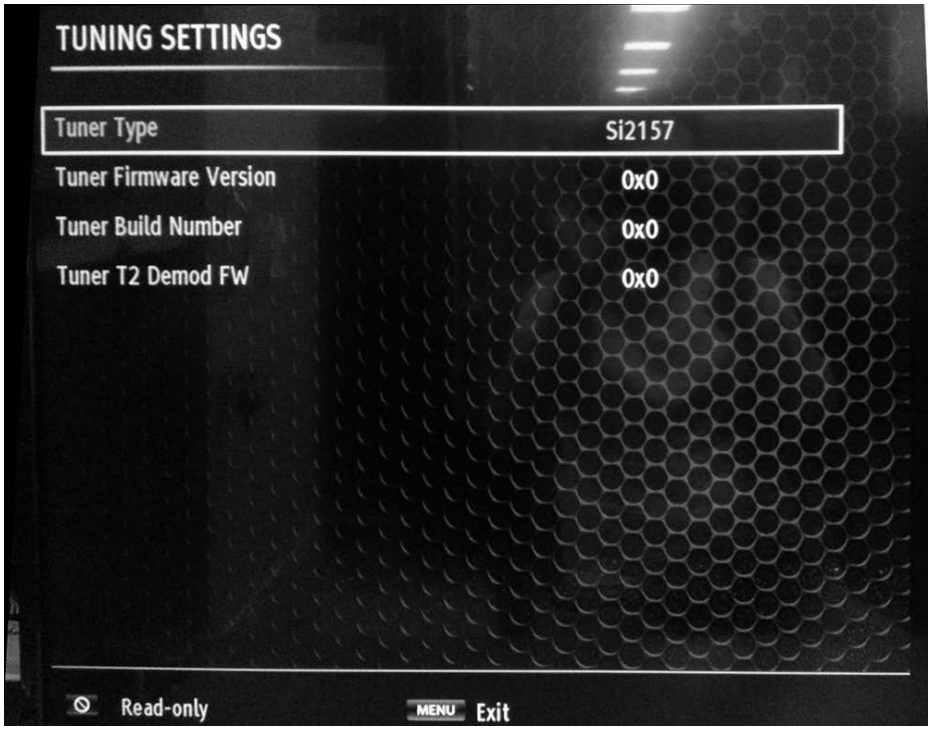
Options-1 Menu



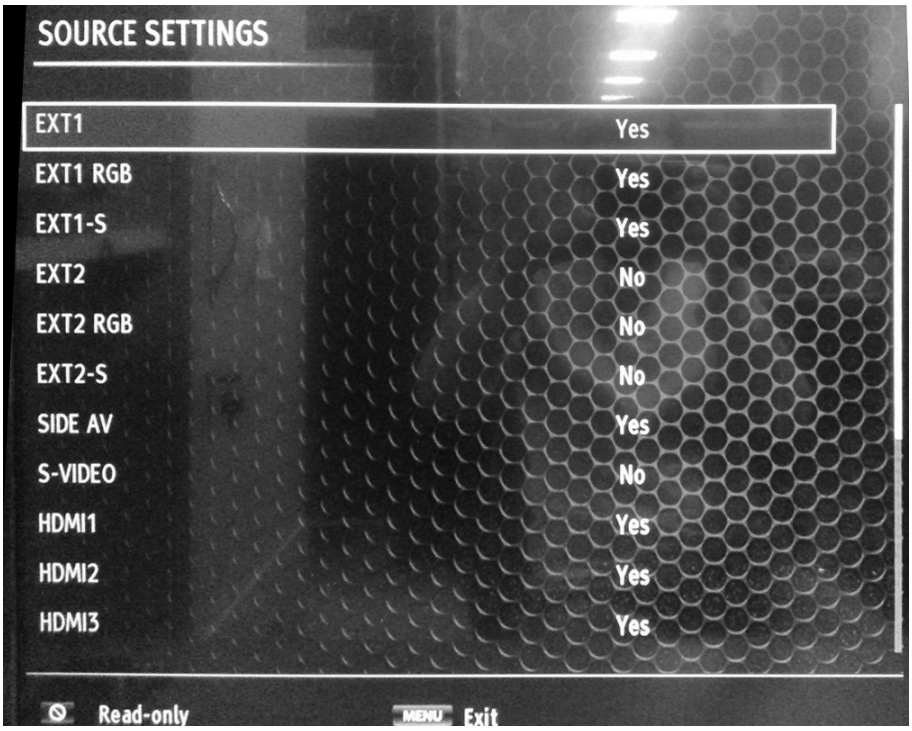
Options-2 Menu



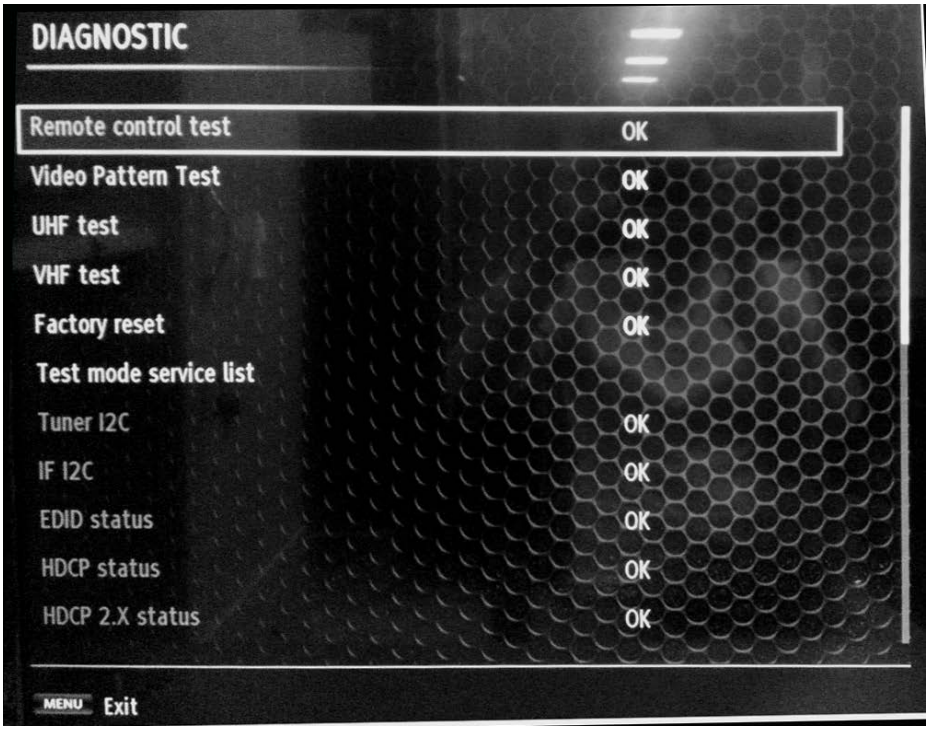
Options-3 Menu



Tuning Settings Menu

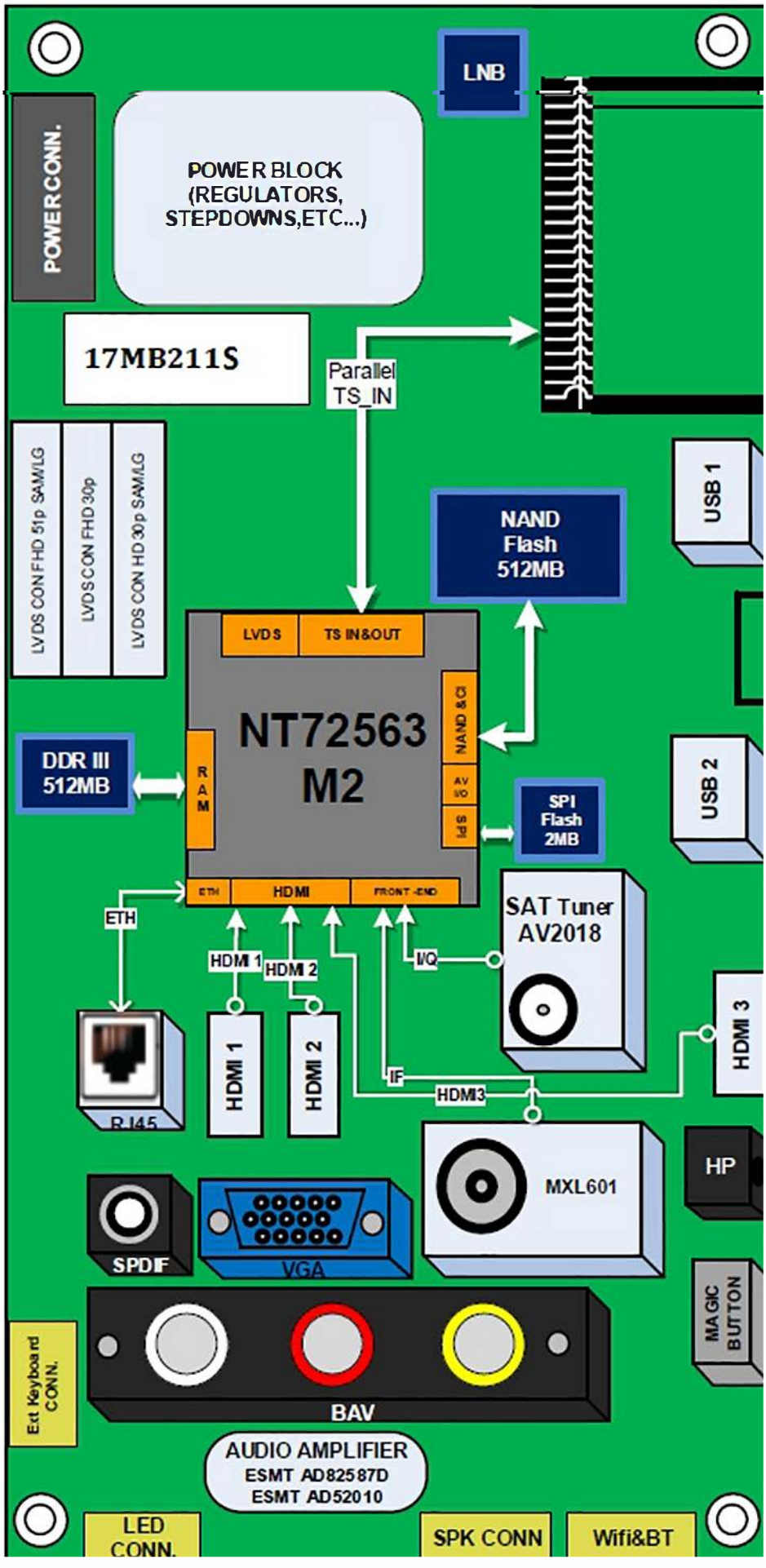


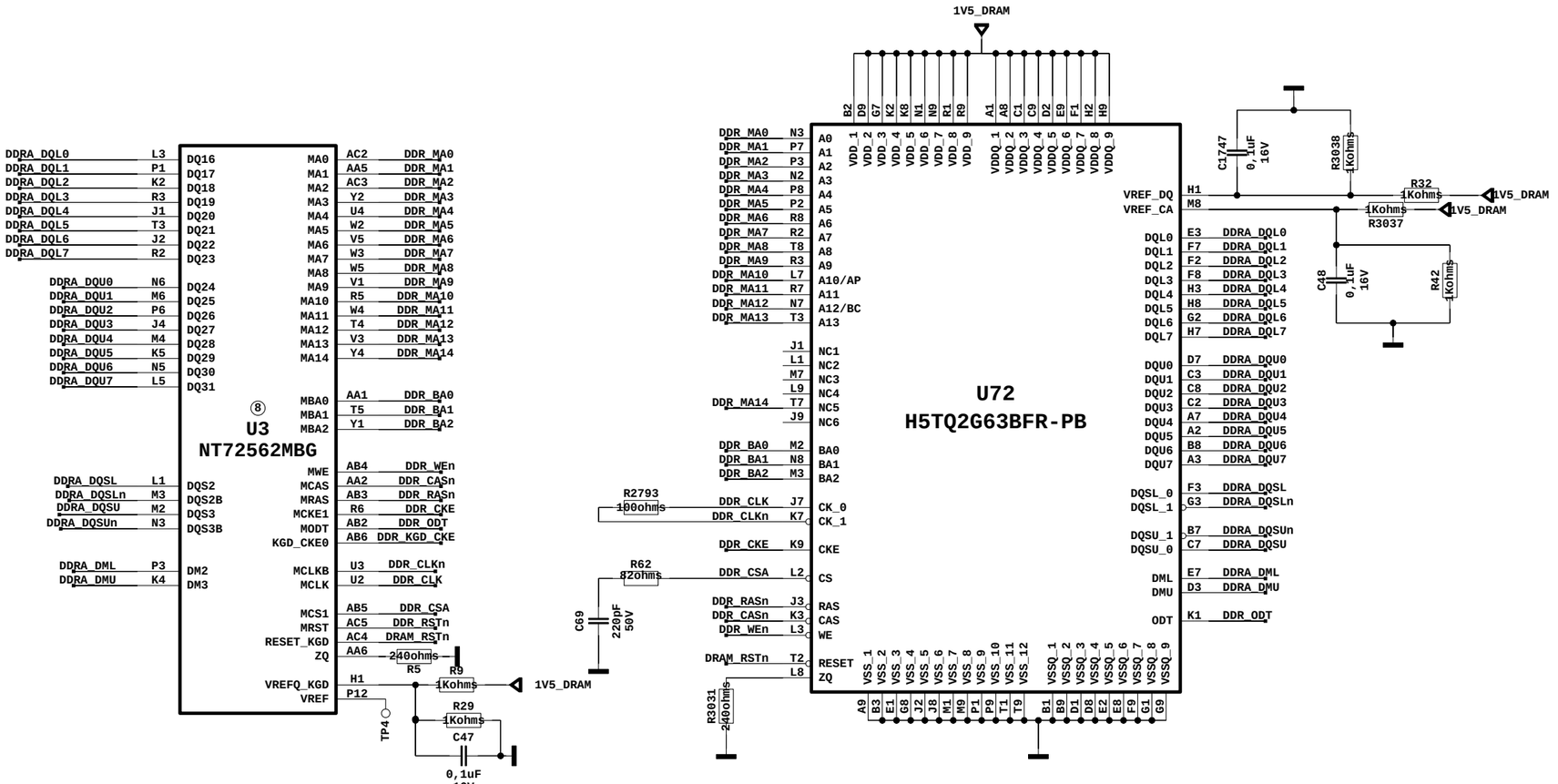
Source Settings Menu



Diagnostic Menu

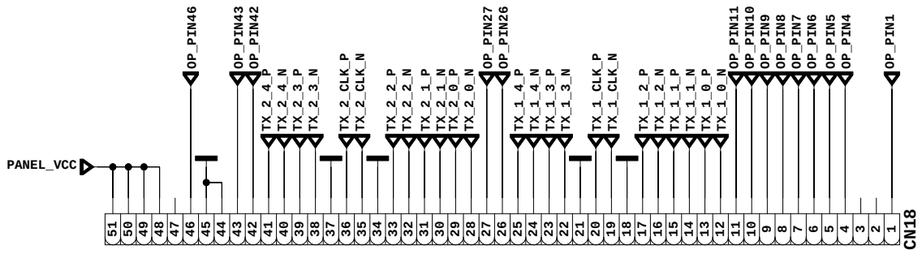
15. GENERAL BLOCK DIAGRAM



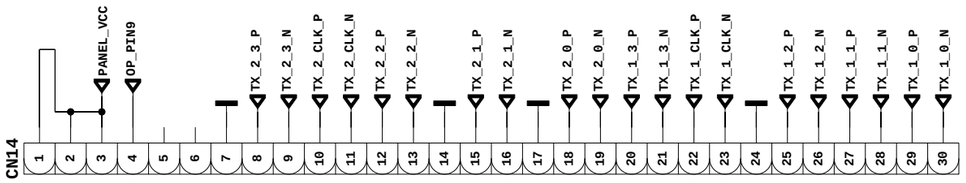


VESTEL	PROJECT NAME 17mb211s-r1	A3
SCH NAME :DDR		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:04

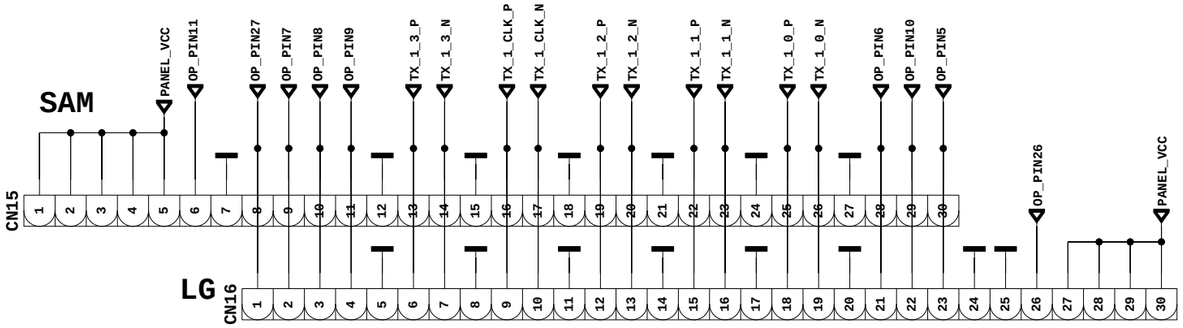
51 PIN FHD



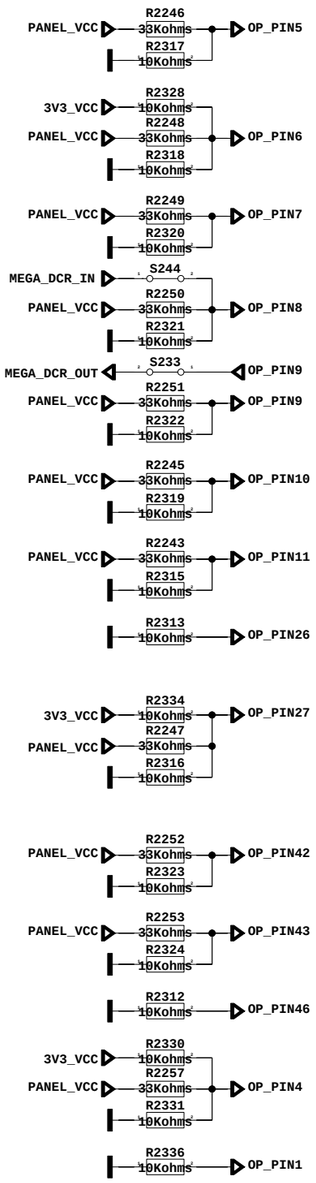
19" TO 22" DOUBLE LVDS FFC OPTIONS



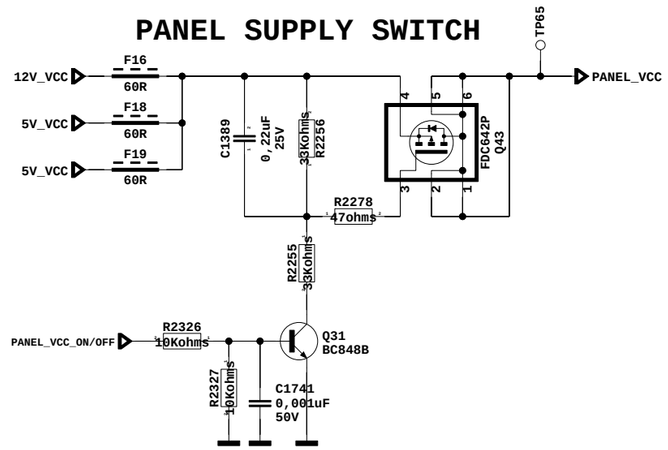
WXGA FFC



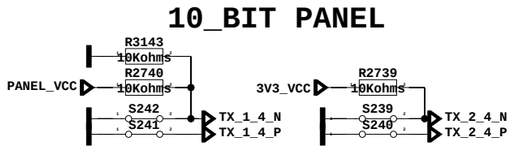
OPTIONS TABLE



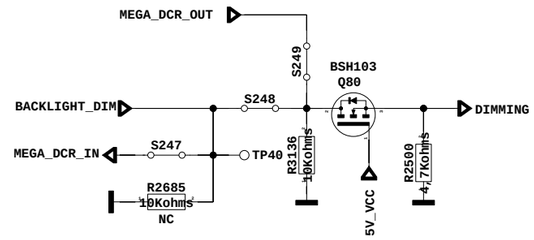
PANEL SUPPLY SWITCH



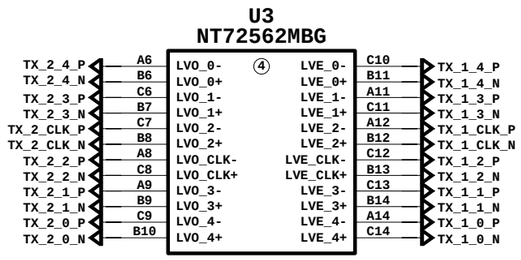
10_BIT PANEL

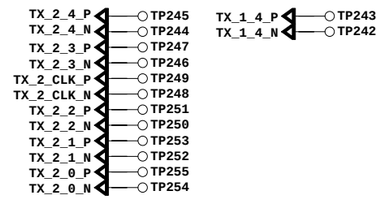


DIMMING

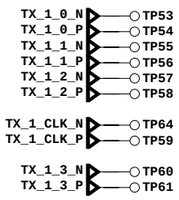


U3
NT72562MBG

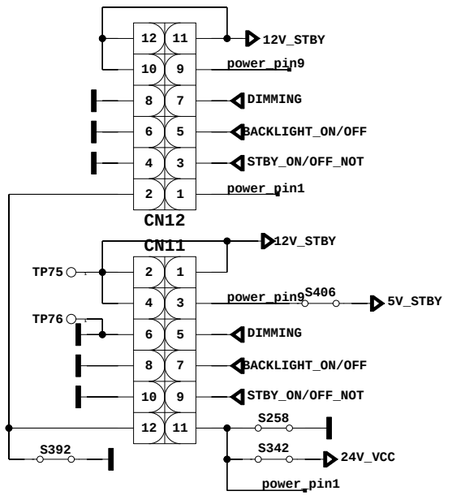




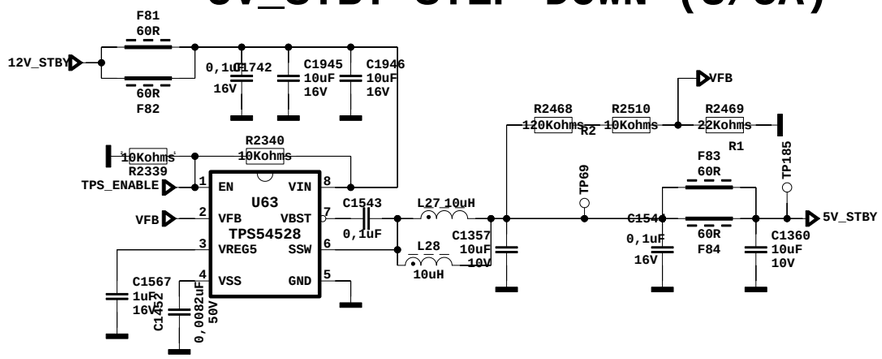
Test Pins



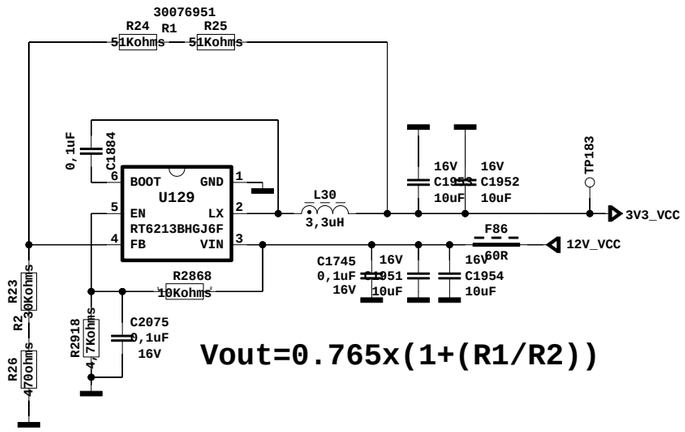
VESTEL	PROJECT NAME :17mb211s-r1	A3
SCH NAME :LVDS		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:04



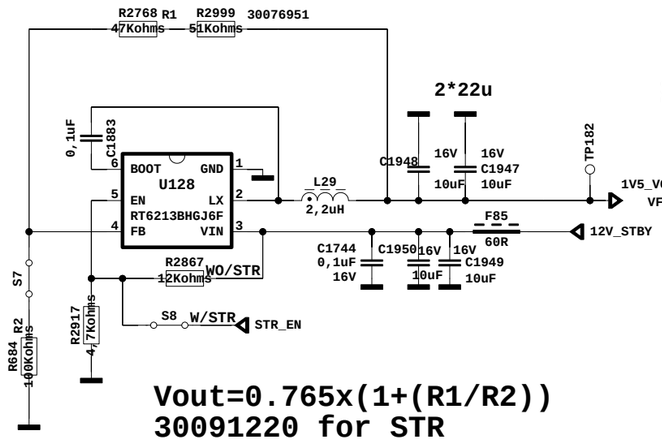
DC/DC 1
5V_STBY STEP-DOWN (3/5A)



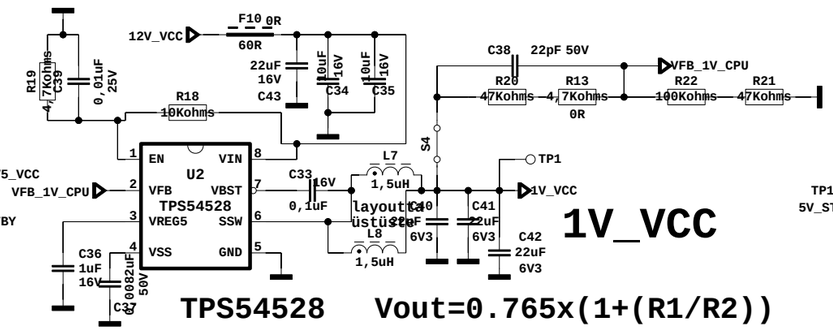
DC/DC 2
3V3_VCC DC/DC (3A)



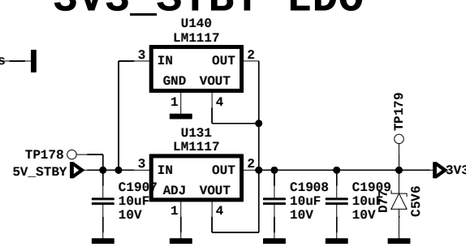
DC/DC 3
1V5_VCC DC/DC (2A)



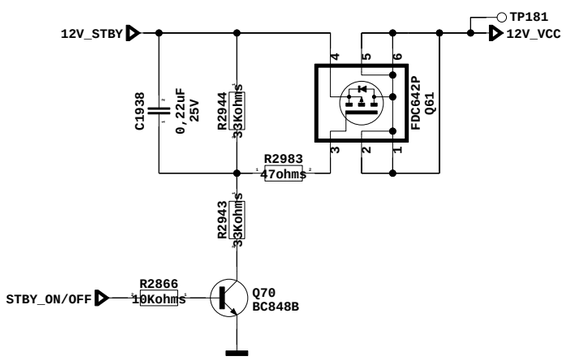
DC/DC 4
1V_VCC DC/DC (5A)



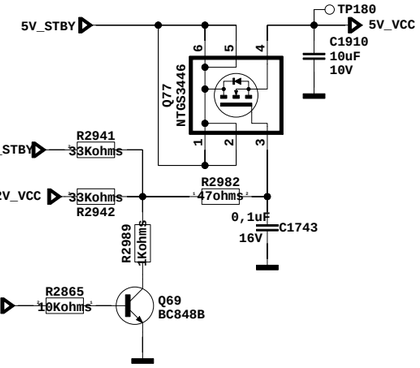
LDO 1
3V3_STBY LDO



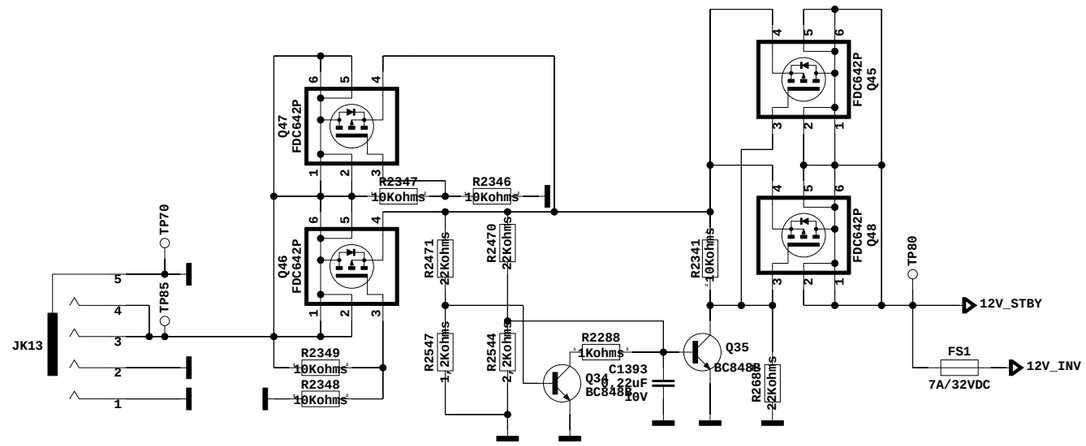
SW1
12V_VCC SWITCH



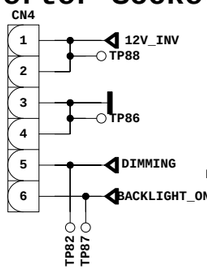
SW2
5V_VCC SWITCH



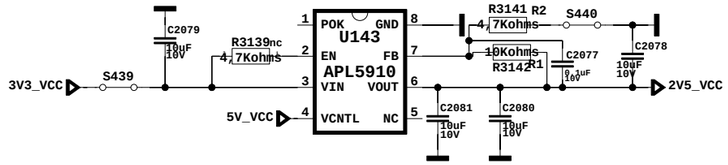
ADAPTER PROTECTION



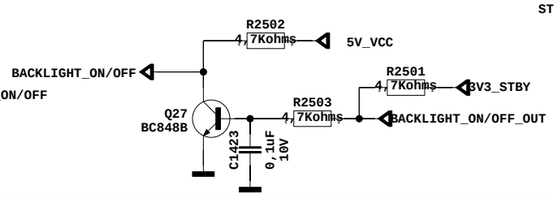
Converter Socket



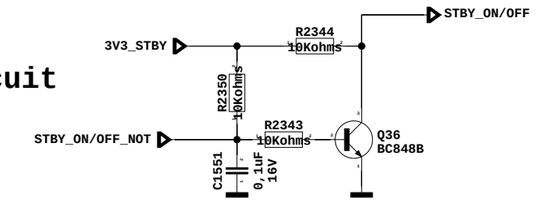
2V5_VCC LDO



Backlight On/Off Circuit



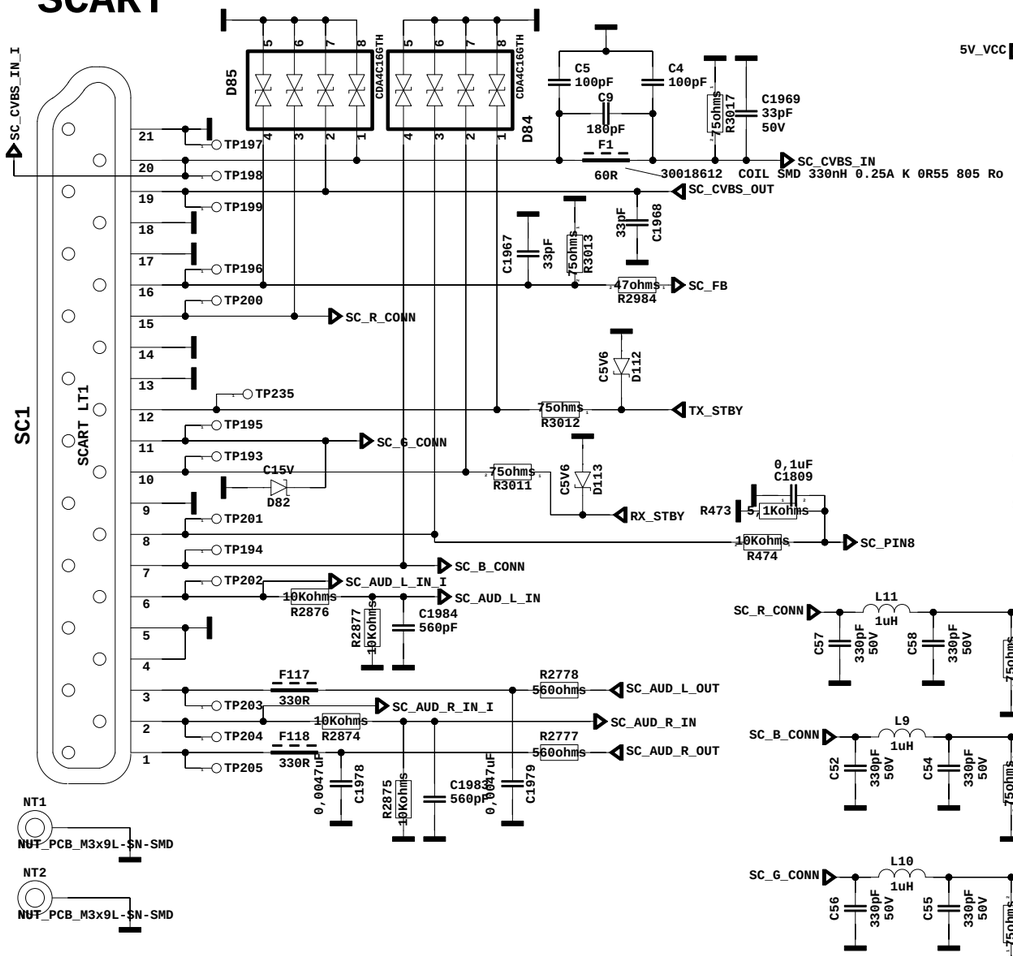
STBY On/Off Circuit



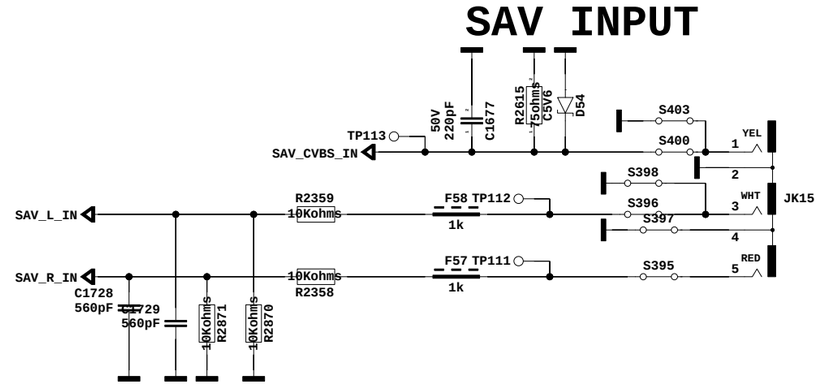
VESTEL	PROJECT NAME :17mb211s-r1	A3
SCH NAME :POWER		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:04

SCART VIDEO OUTPUT AMPLIFIER

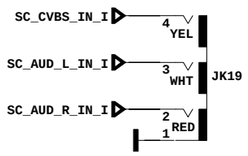
SCART



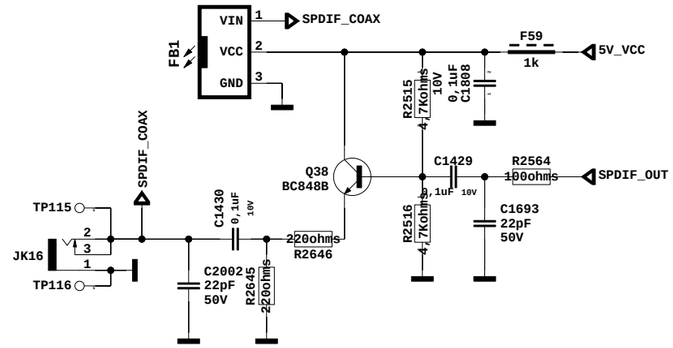
SAV INPUT



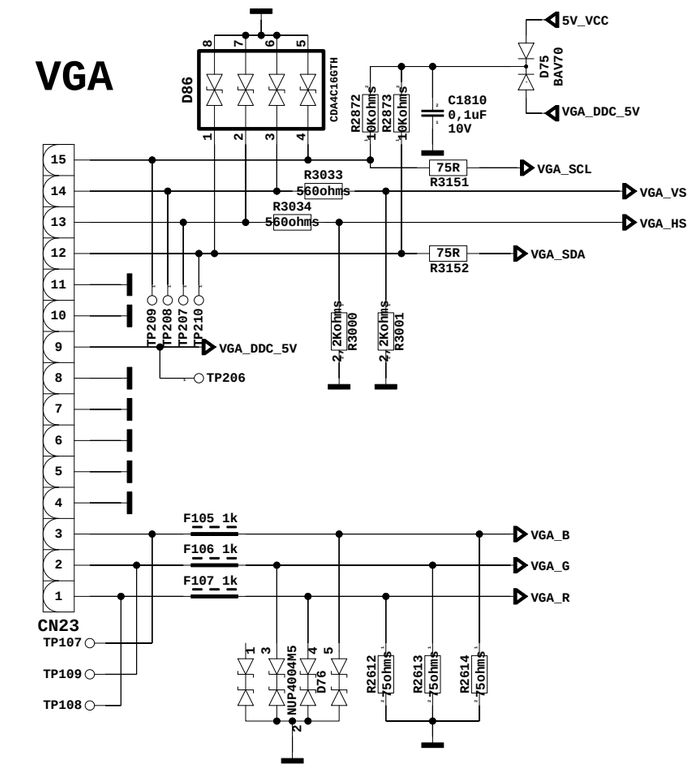
INDIA OPTION



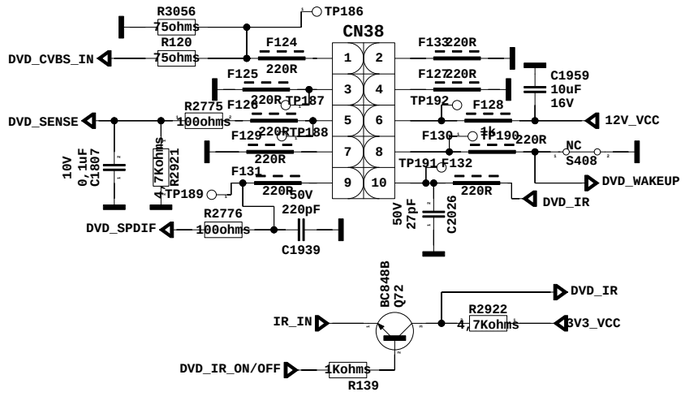
SPDIF OUT



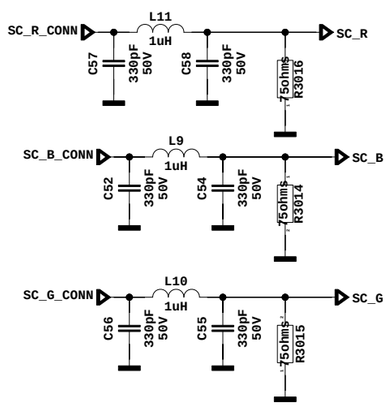
VGA



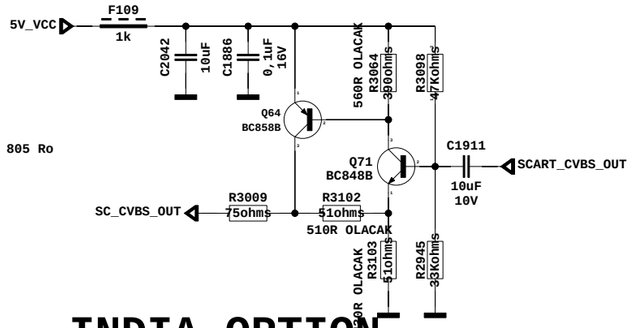
DVD INTERFACE



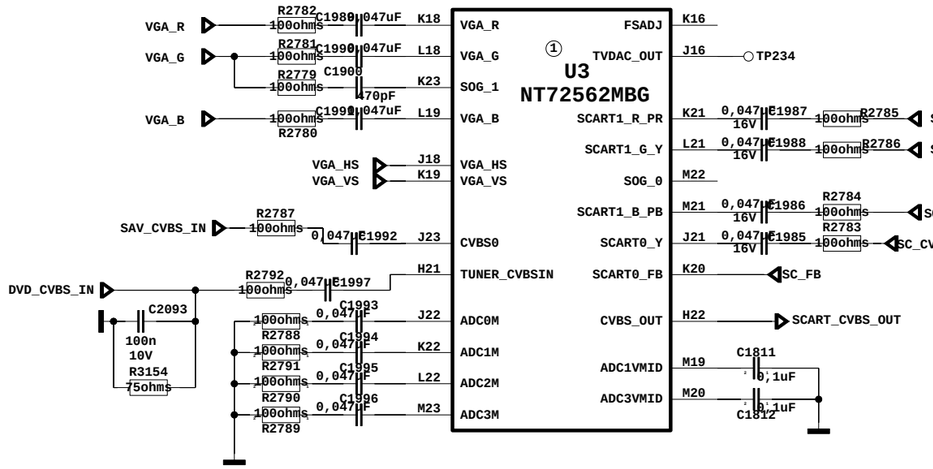
SC_R_CONN / SC_B_CONN / SC_G_CONN



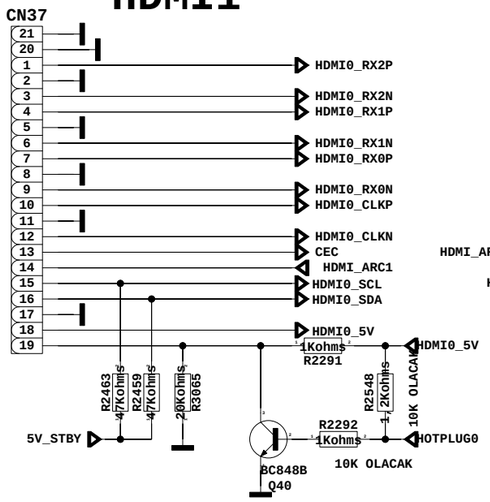
5V_VCC / SC_CVBS_OUT

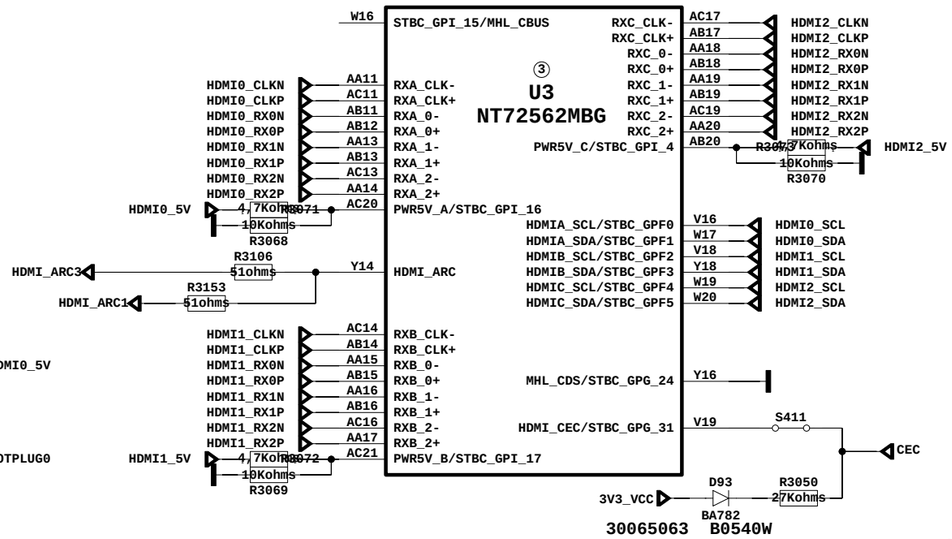


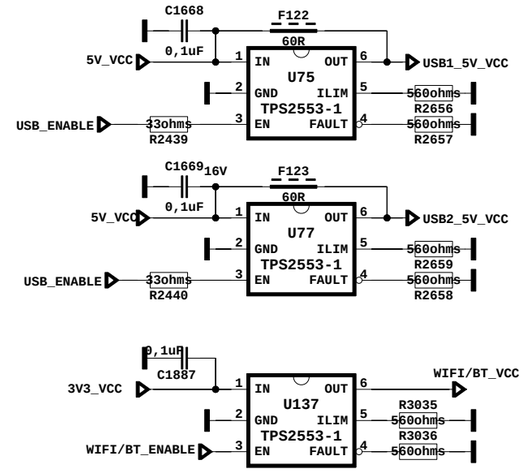
U3 NT72562MBG

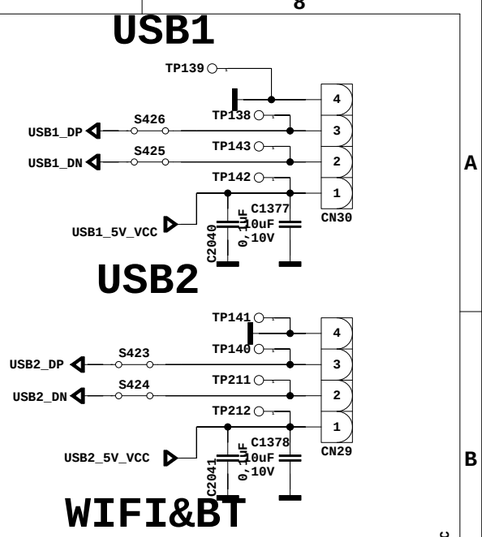


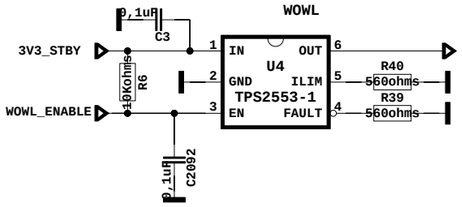
VESTEL	PROJECT NAME 17mb211s-r1	A3
SCH NAME :PERIPHERALS		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05

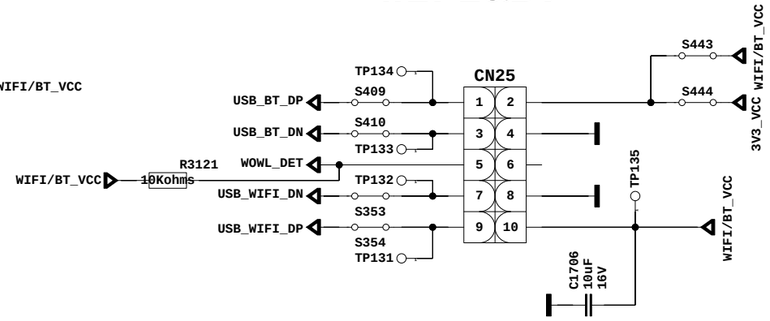


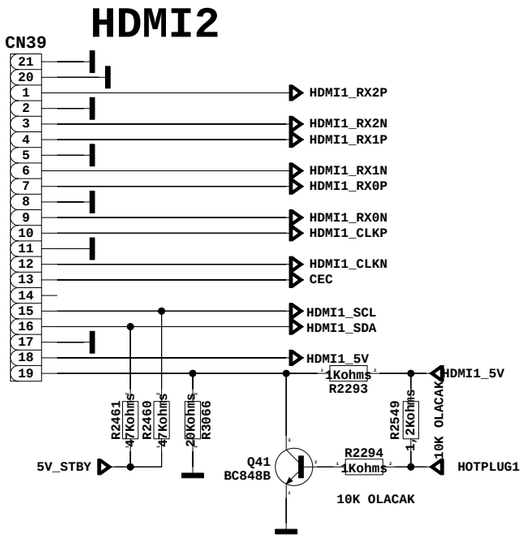


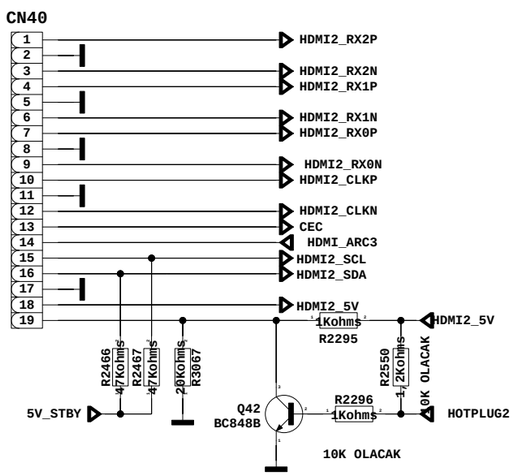


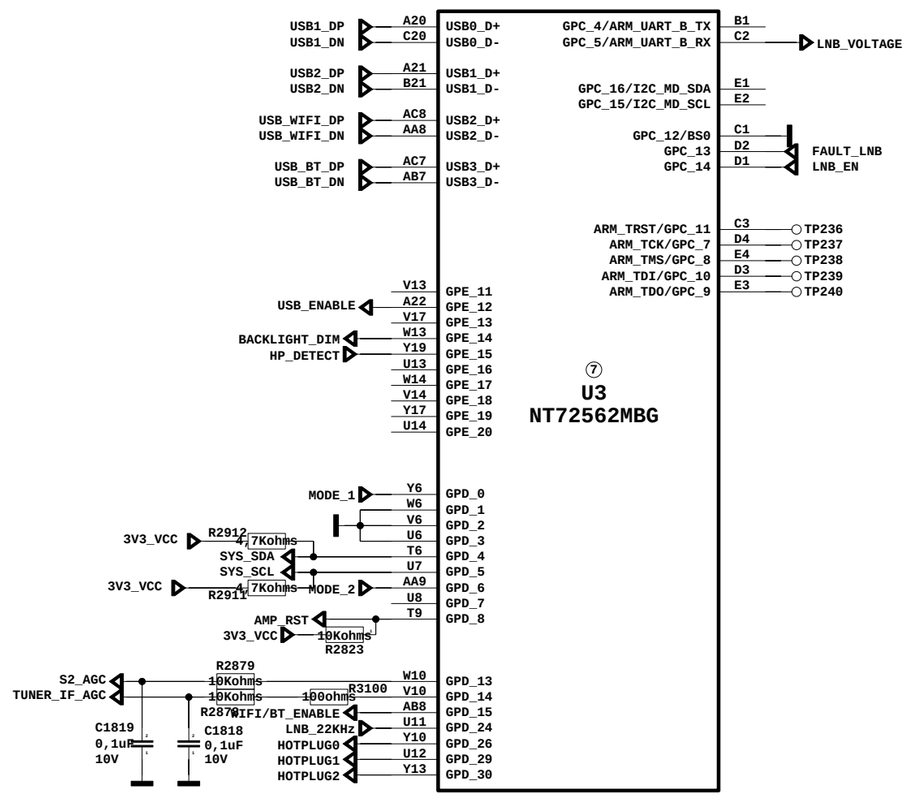










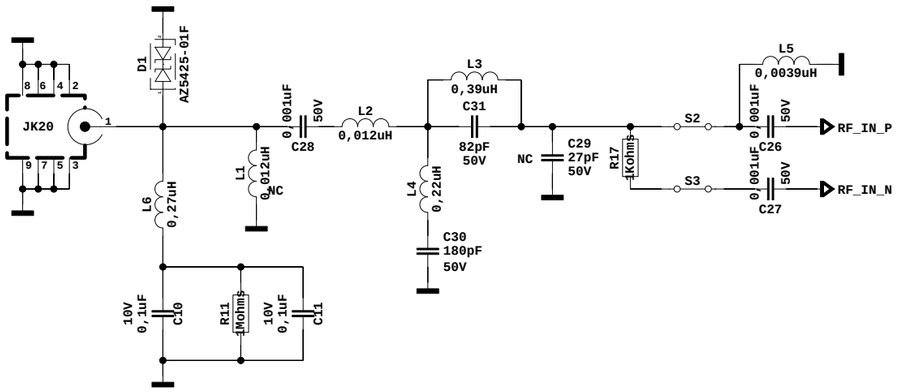


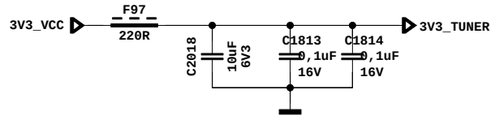
CLOSE TO IC SIDE

S2_AGC VE TUNER_OF_AGC COMPONENTS

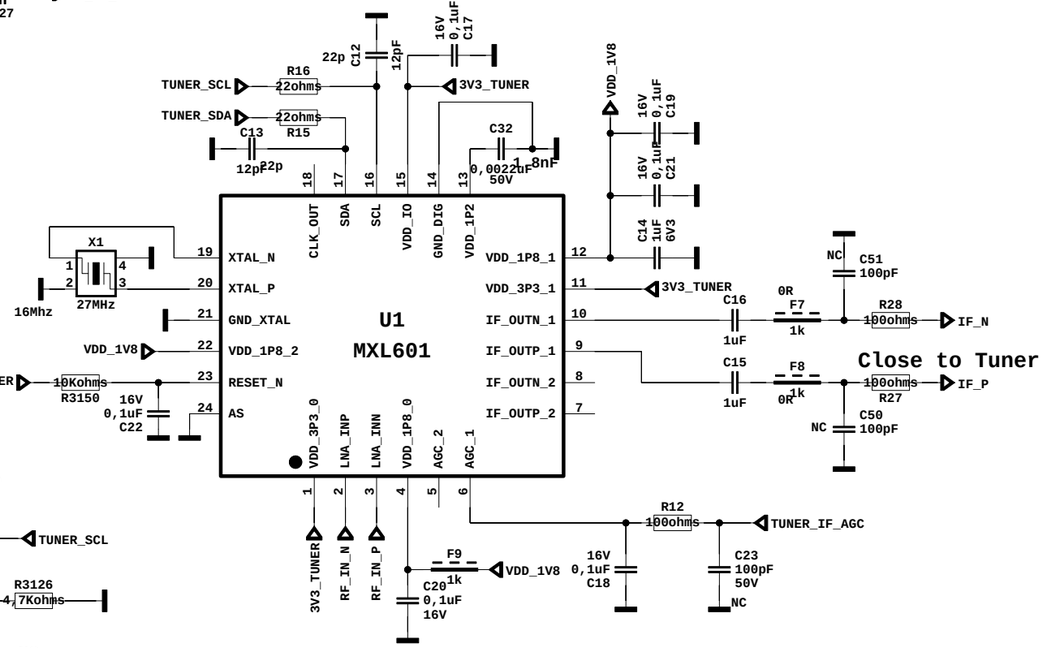
VESTEL	PROJECT NAME : 17mb211s-r1	A3
SCH NAME :HDMI_USB_NT72670_PWR		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05

TUNER

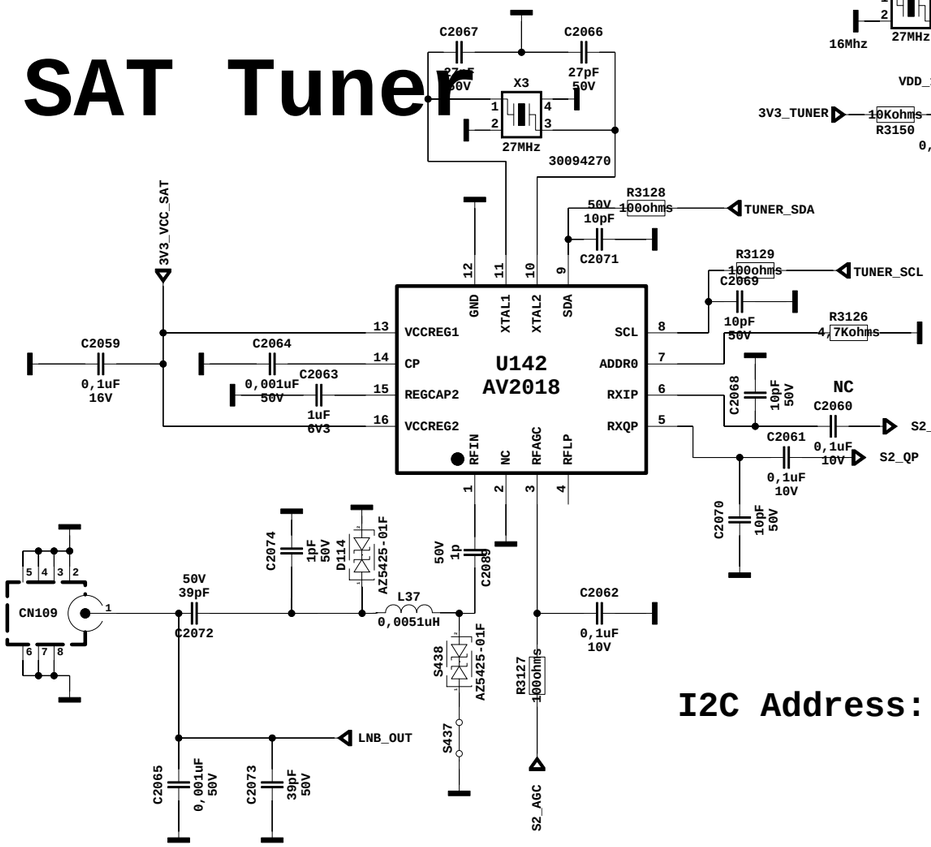




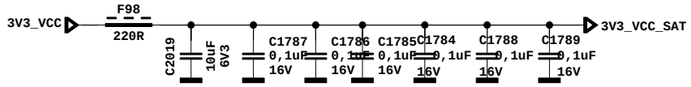
TUNER



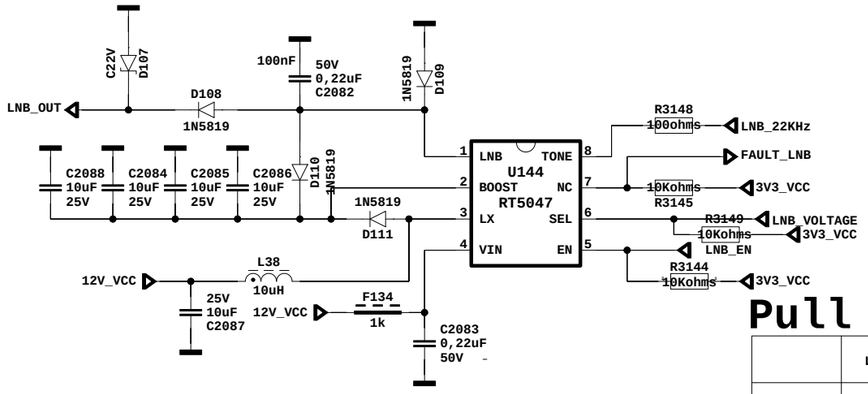
SAT Tuner



I2C Address: C4



LNBP

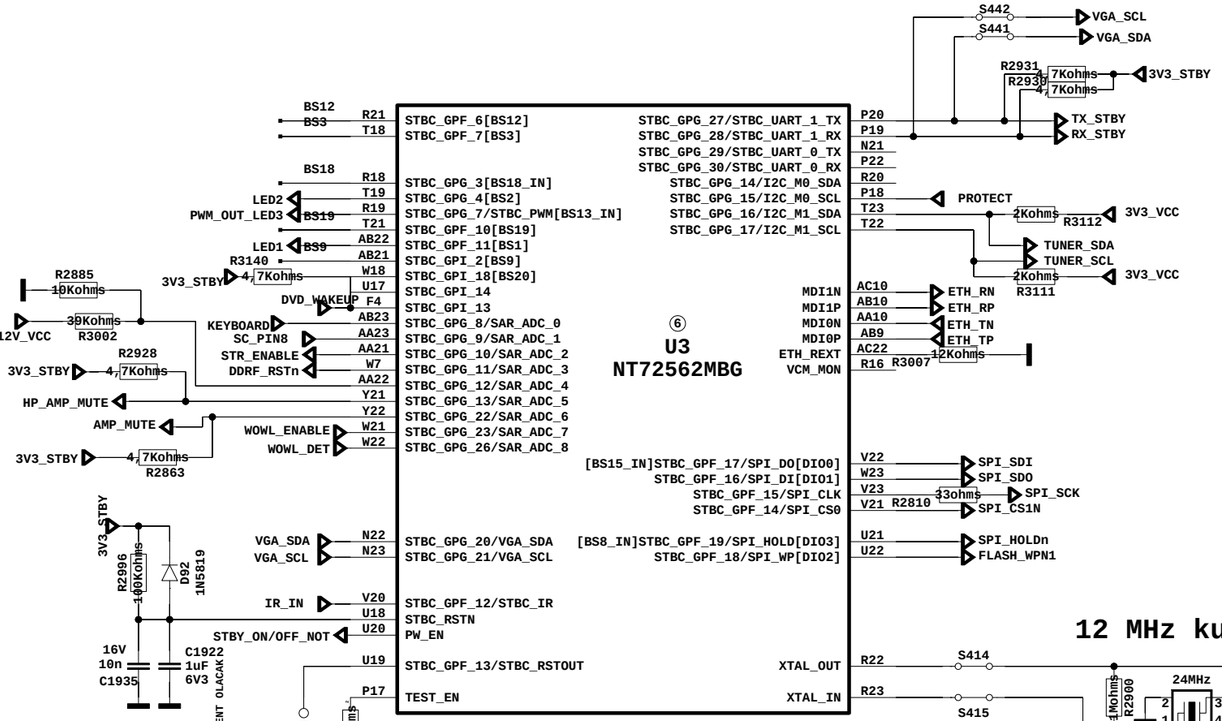


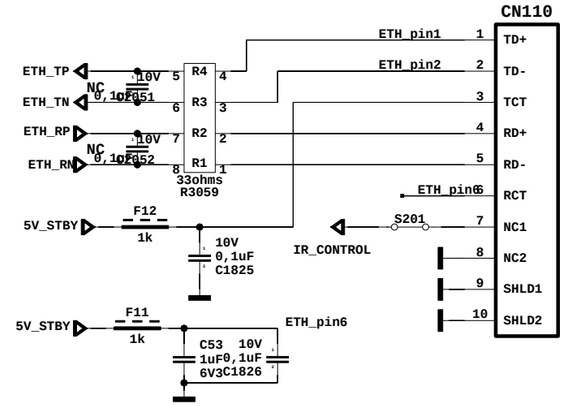
Pull up/Pull down

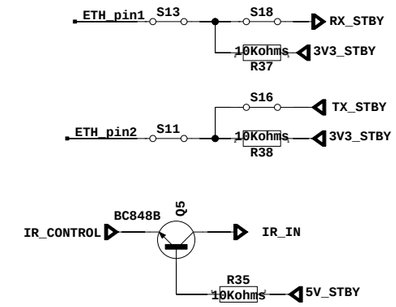
	LNB_VOLTAGE	LNB_EN
HIGH	18V	ENABLE
LOW	13V	DISABLE

VESTEL	PROJECT NAME : 17mb211s-r1	A3
SCH NAME :TUNER_SAT_LNB		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05

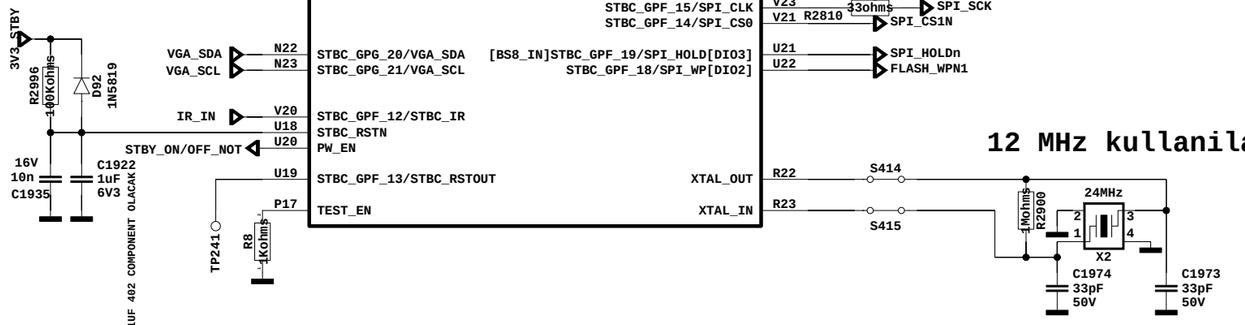
ETHERNET



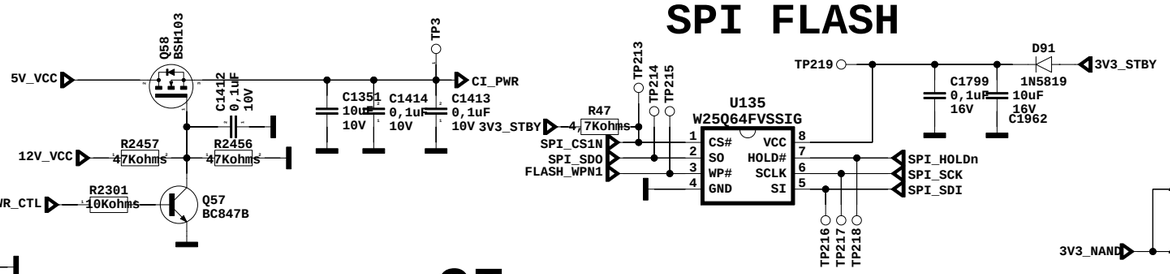




12 MHz kullanilacak. (30068172)



SPI FLASH



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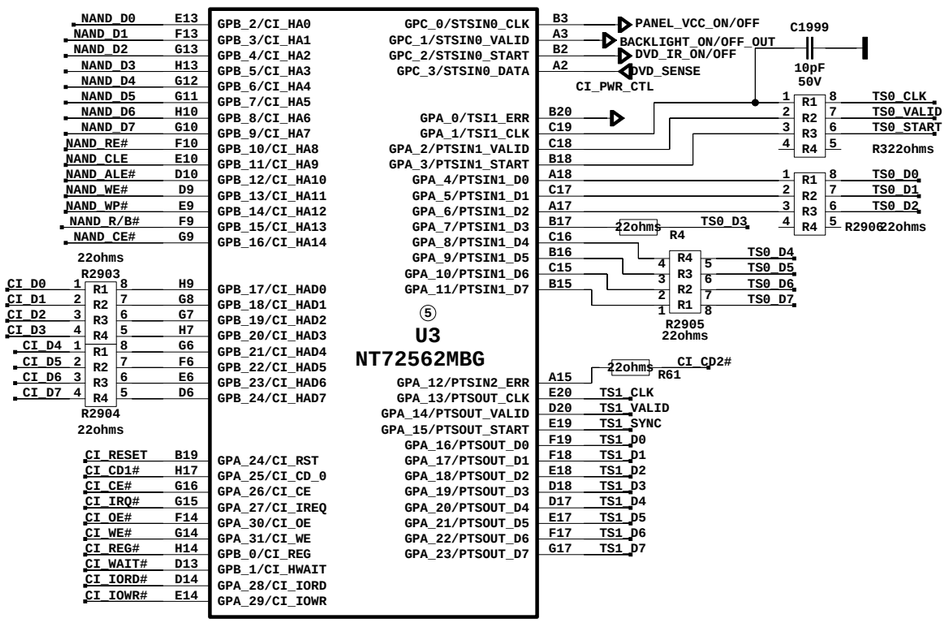
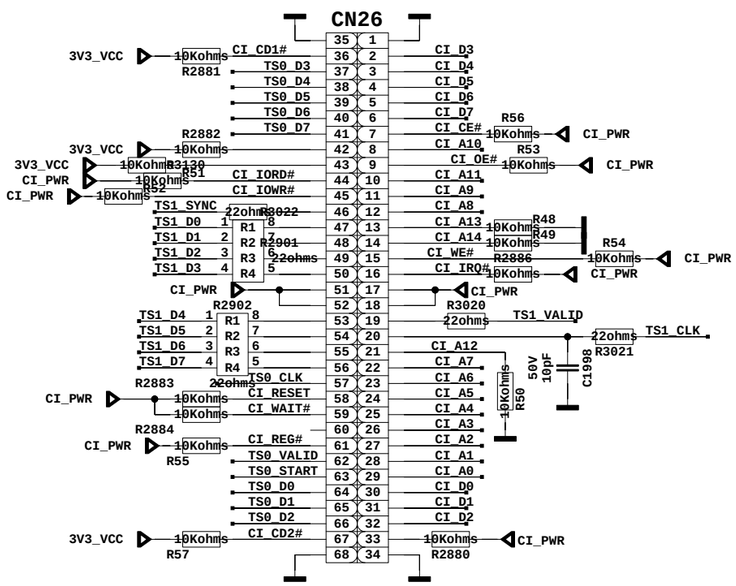
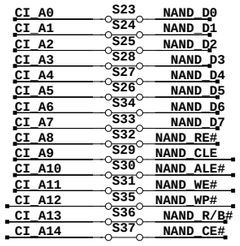
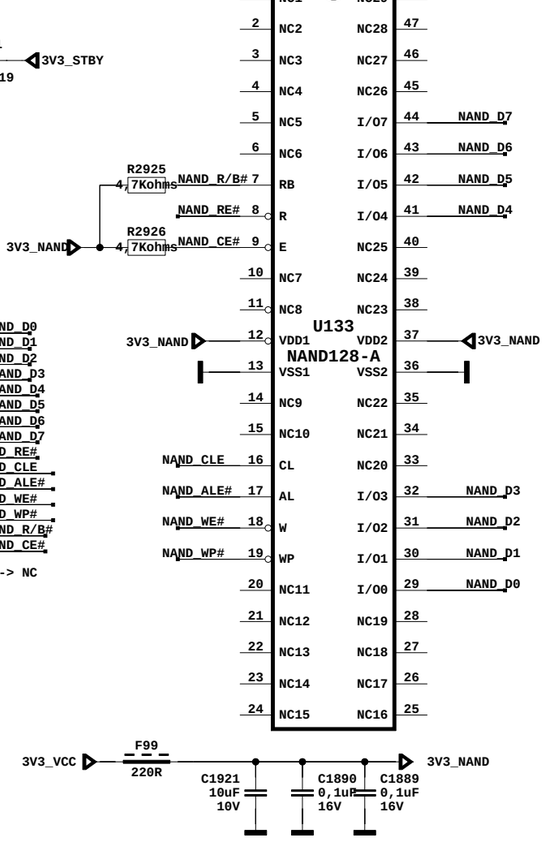




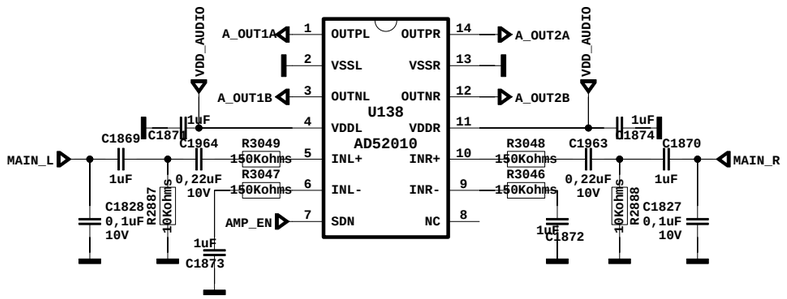


NAND FLASH

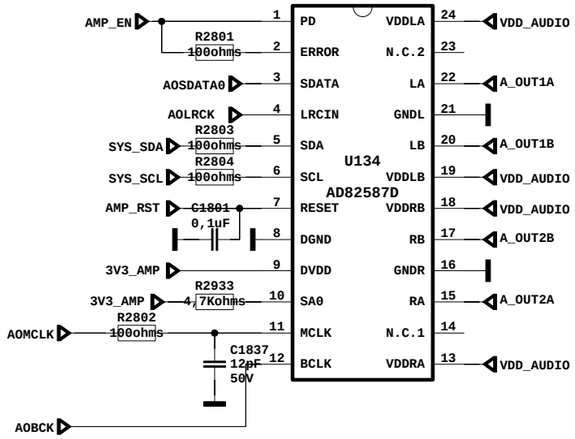


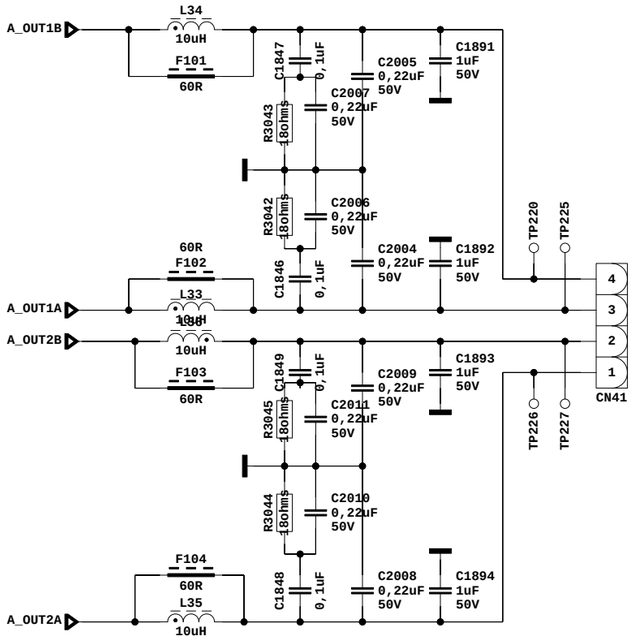
VESTEL	PROJECT NAME : 17mb211s-r1	A3
	SCH NAME :CI_NAND_SPI_ETH	T. SHT 10
	DRAWN BY :<YOUR NAME HERE>	23/08/2017:17:05

2W5 OPTION

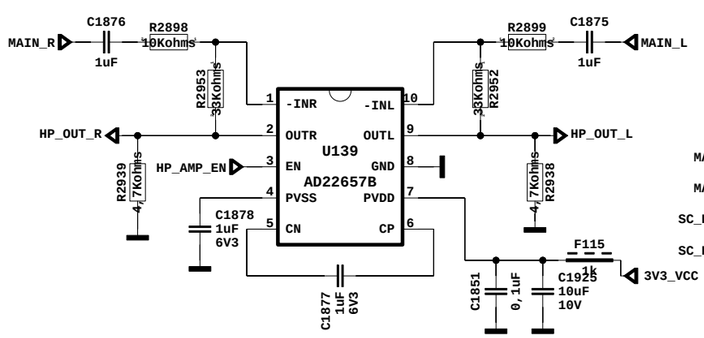


6W/8W/10W OPTION





HEADPHONE AMP



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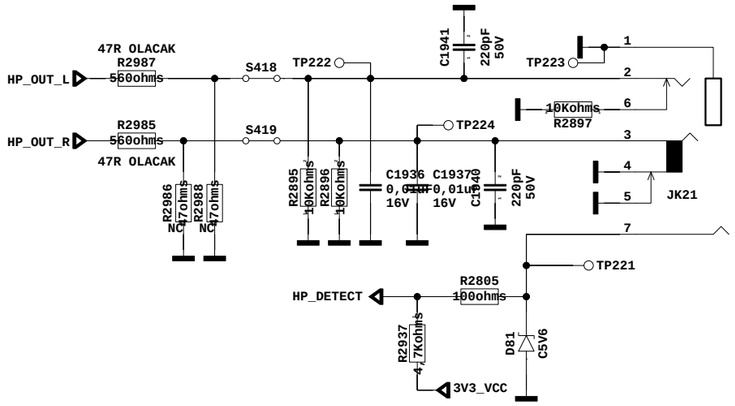
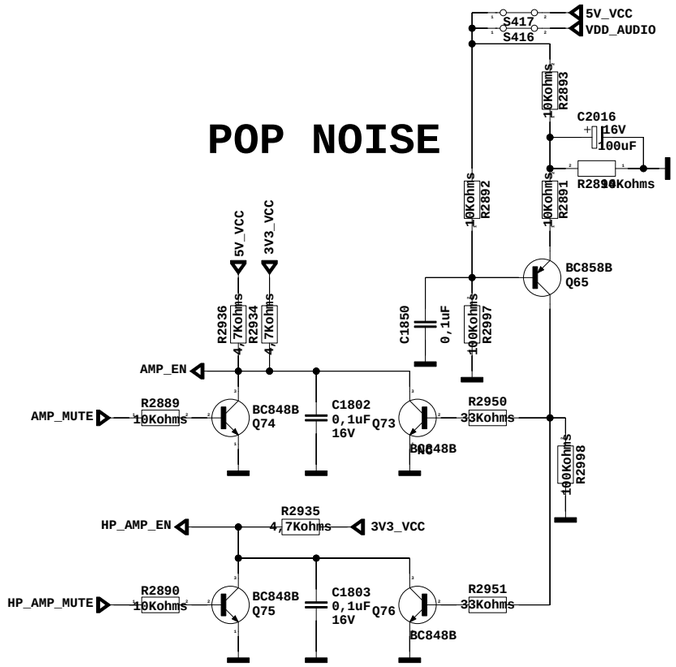
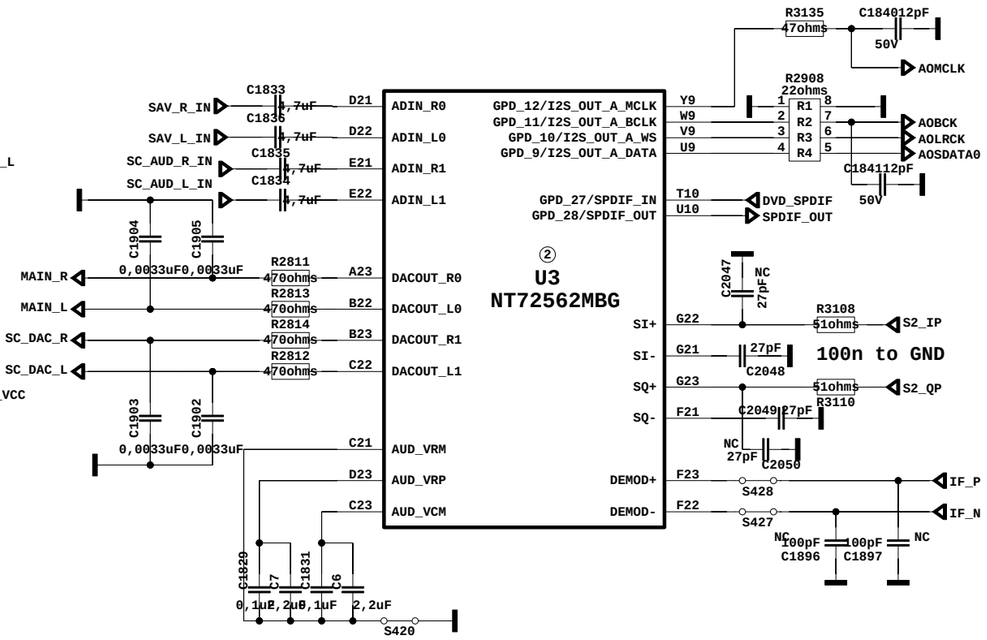


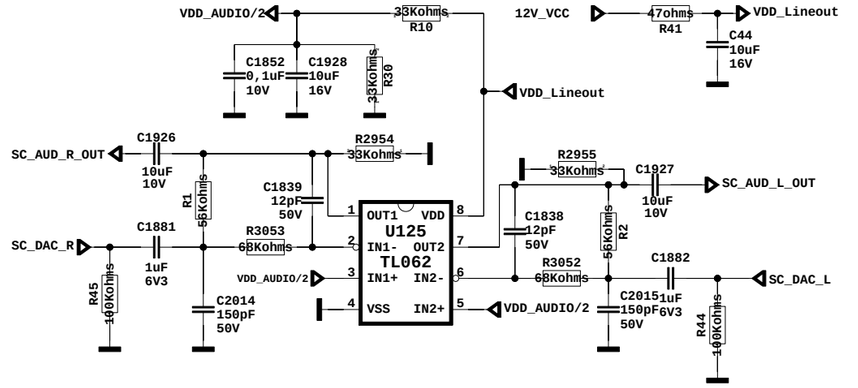
POP NOISE



HEADPHONE AMP

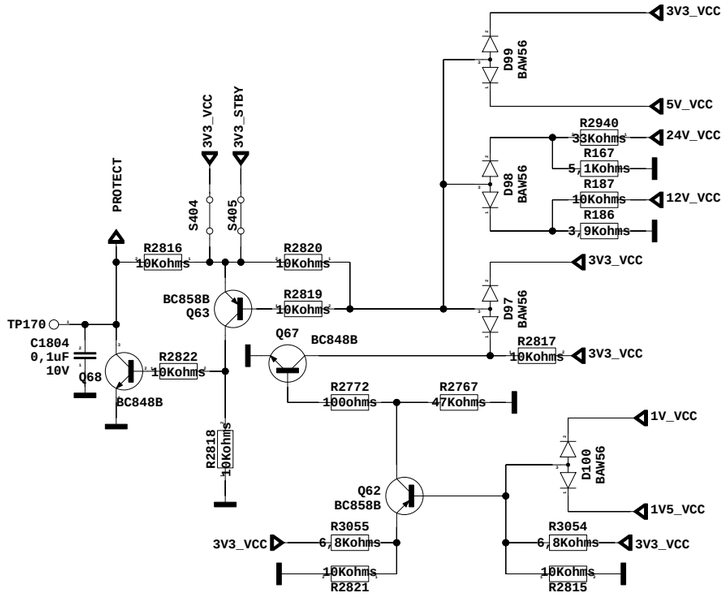


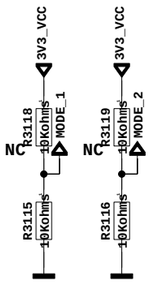
SCART AUDIO AMP

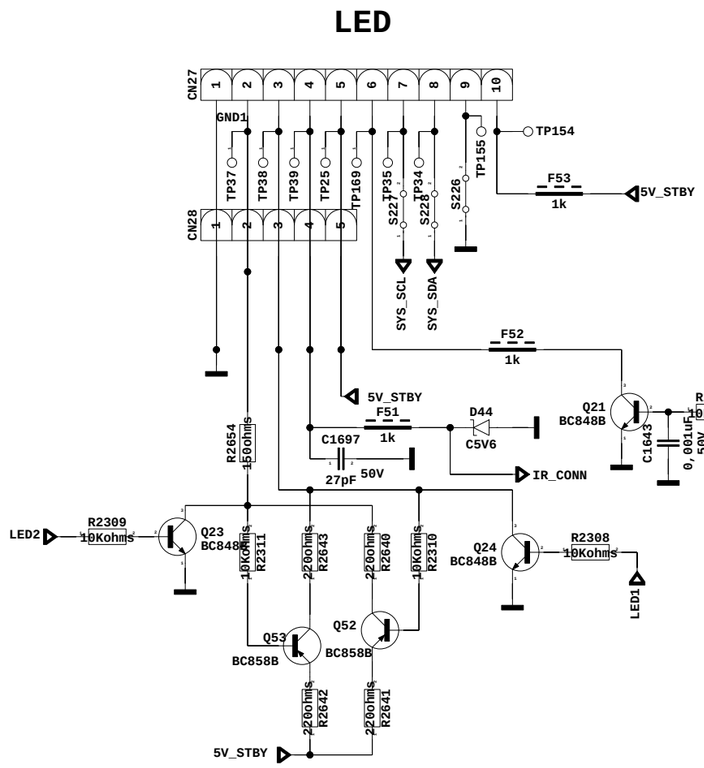


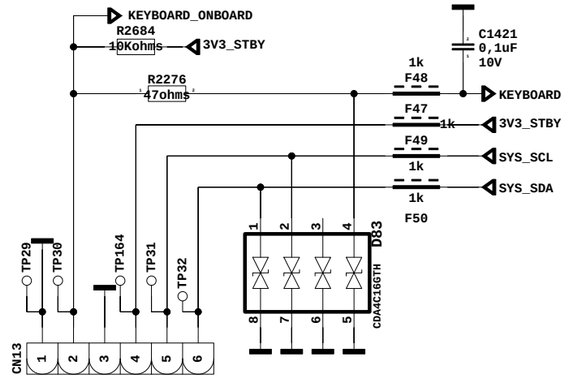
VESTEL	PROJECT NAME 17mb211s-r1	A3
SCH NAME :AUDIO AMPs		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05

PROTECTION

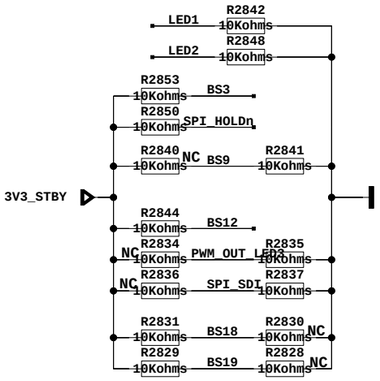




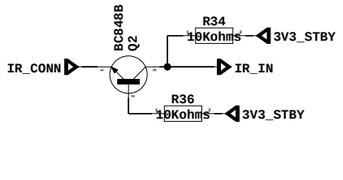


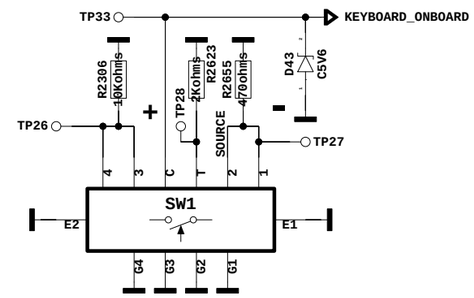


KEYBOARD

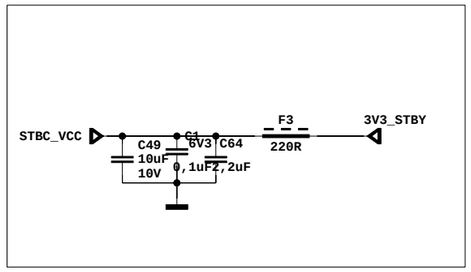


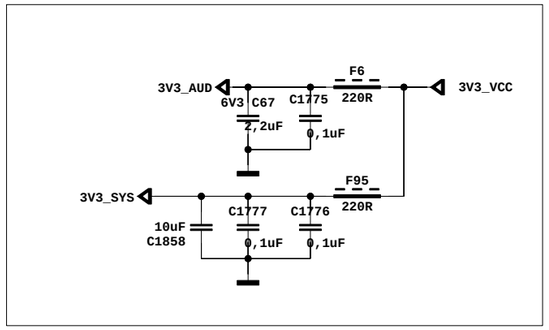
3-WAY

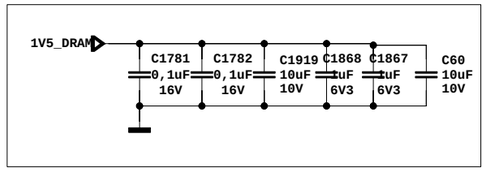


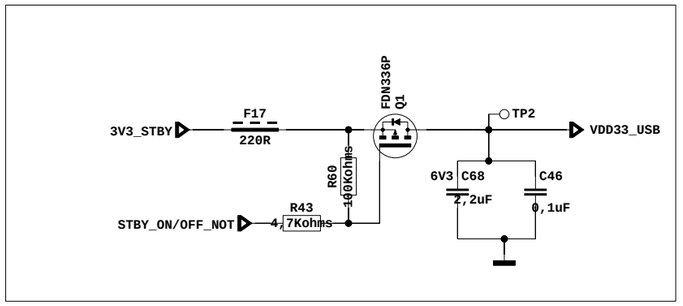


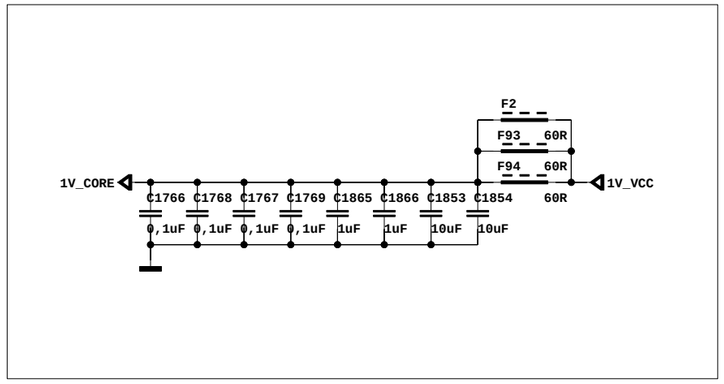
VESTEL	PROJECT NAME : 17mb211s-r1	A3
SCH NAME :GPIOs		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05

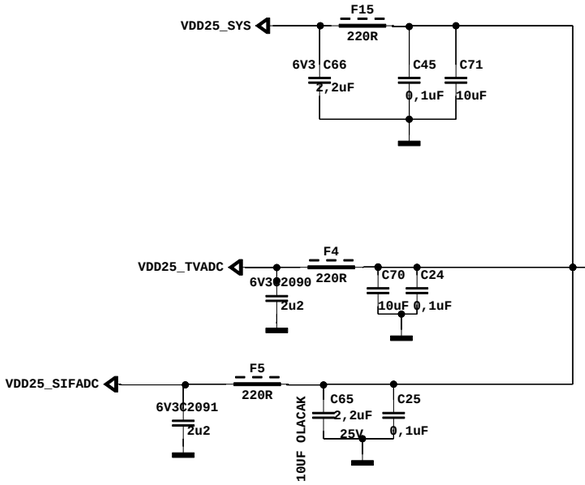


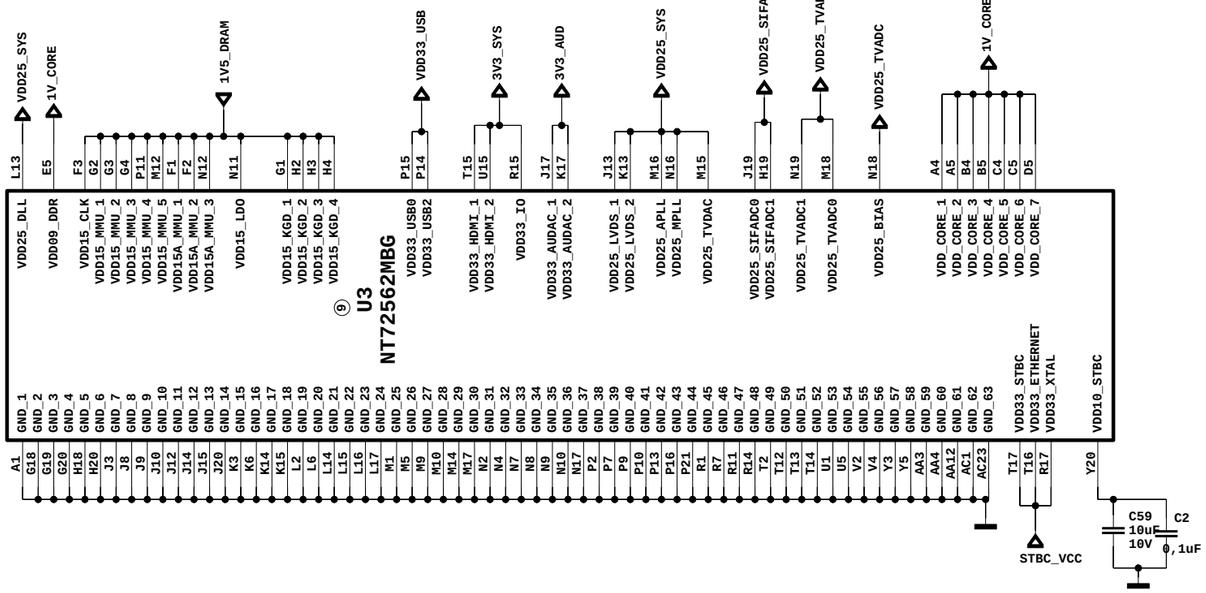












VESTEL	PROJECT NAME : 17mb211s-r1	A3
SCH NAME :NT72562_POWER		T. SHT 10
DRAWN BY :<YOUR NAME HERE>		23/08/2017:17:05