MB181TC IDTV
SERVICE MANUAL

Table of Contents

IMPORTANT
Before removing the rear cover from the TV for servicing, make sure that no cables are fixated to the cover. Release the cables from their clamps and disconnect (if any). Failure to do so may damage the wires and/or other components of the TV.

1. INTRODUCTION

17MB181TC main board is driven by MTK SOC. This IC is a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.

This board can be driven just 50Hz HD and FHD panels.

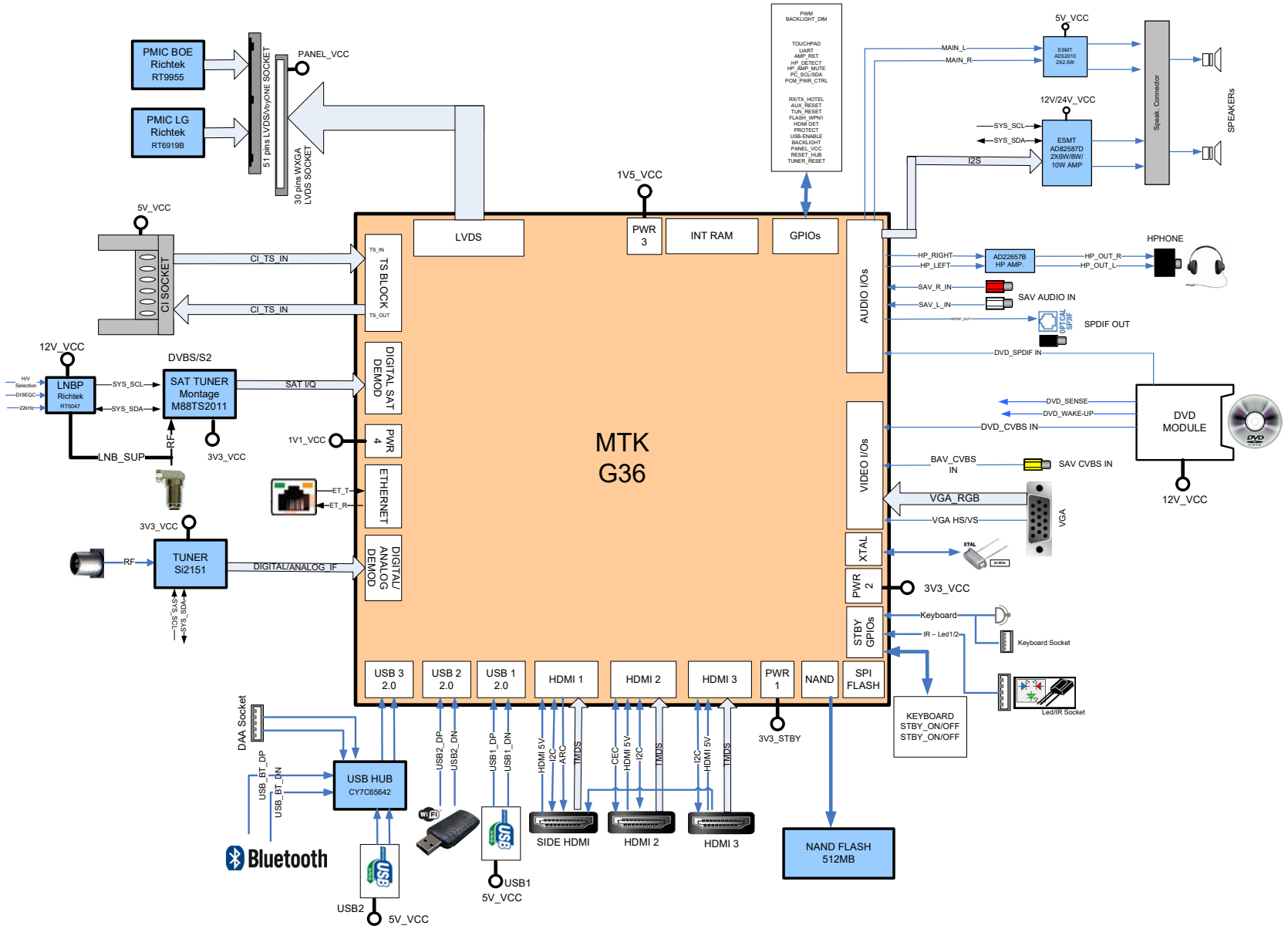
Key features include:

- Combo Front-End Demodulator
- A multi standart A/V format decoder
- The MACEpro video processor
- Home theatre sound processor
- Rich internet connectivity and completed digital home network solution
- Dual-stream decoder for 3D contents
- Mılti-purpose CPU for OS and multimedia
- Peripheral and power management
- Embedded DRAM (for connected option)

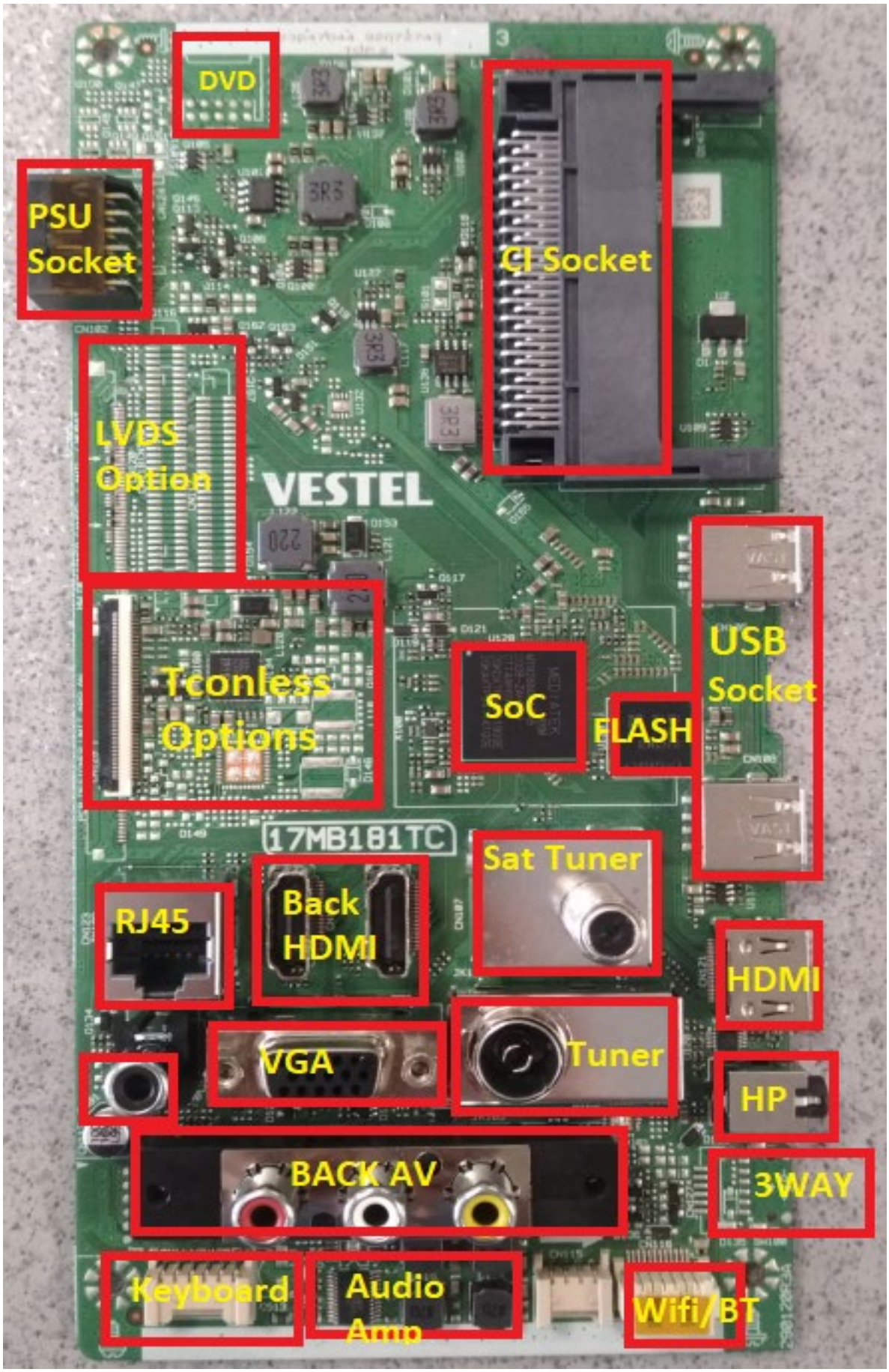
Supported peripherals are:

- 1 RF input VHF I, VHF III, UHF
- 1 Satellite input
- 1 Back AV (CVBS, R/L_Audio)
- 1 YPbPr (from VGA with special cable) (Optional)
- 1 PC input(Common)
- 2xBack HDMI 1x Side HDMI input (with ARC option from 2nd input)
- 1 Common interface(Common)
- 1 Optic/ Quax S/PDIF output
- 1 Headphone(Common)
- 2 USB(1X Side Common, 1X Side Optional) and 2x internal USB for Wifi/Bluetooth
- 1 Ethernet-RJ45
- 1 3way/External Touchpad/Tact Switch (Common)
- 1 Internal DVD module support

A.GENERAL BLOCK DIAGRAM



B. PLACEMENT OF BLOCKS



2. T/T2/C/A TUNER (U118)

Description

The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.

Features:

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVBT2/T/C2/C, ISDB-T/C, DTMB
- 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
- 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™,DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V singlesupply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant

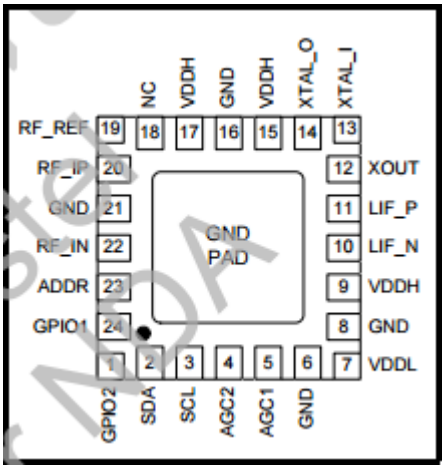


Figure 1: Si2151 Pin description

Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I^2C data input/output
3	SCL	I	I^2C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground

17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I^2C address select
24*	GPIO1	I/O	General purpose input/output #1
***Note:** Pin should be left floating if unused.			

Table 1 Si2151 Pin function

3. S/S2 TUNER (U136) OPTIONAL

Description

M88TS6011 is a single chip, direct-conversion tuner for digital satellite receiver applications. Its offers the industry's most integrated solution to a satellite tuner function, simplifying the front-end design. This device incorporates the following function blocks on a single chip: an LNA, quadrature down-converting mixers, a low phase noise and fast locking frequency synthesizer with on-chip loop filters, a DC offset cancellation loop with integrated loop filters, self-calibrated programmable baseband channel filters, an integrated RF AGC loop, and crystal oscillators with and integrated auxiliary clock output.

As a result of integrating all these blocks, the M88TS6011 has the least number of pins compared with other conventional solutions, and requires the least external compopnents. In typical applications, M88TS6011 requires only one crystal, one matching network, and a few external capacitors. The device also has the industry's smallest latency, as it uses a fast locking PLL and fast settling DC offset cancellation architecture.

The M88TS6011 can be configured via a 2-wire serial bus. The chip is available in a 16-pin QFN package.

Features

- Single-Chip tuner
- Compliant with DVB-S2 and ABS-S standards
- Support QPSK, 8PSK, 16APSK AND 32APSK
- Direct-conversion from L-band to baseband
- Symbol rate:1 to 45 Msybol/s
- Integrated VCOs and PLL, with on-chip inductors varactors and loop filter
- Integrated baseband filters: 6 MHz to 40 MHz bandwith
- Integrated RF AGC for optimal performance
- Integrated baseband DC offset cancellation removes external loop filters
- Excellent immunity to strong adjacent undersired channels
- Integrated clock driver provides auxiliary divided clock output for other devices
- Support sleep mode
- 2-wire serial bus with 3.3V compatible logic levels

- Power supply: +3.3V
- Package: 16-pin E-PAD QFN
- RoHS compliant

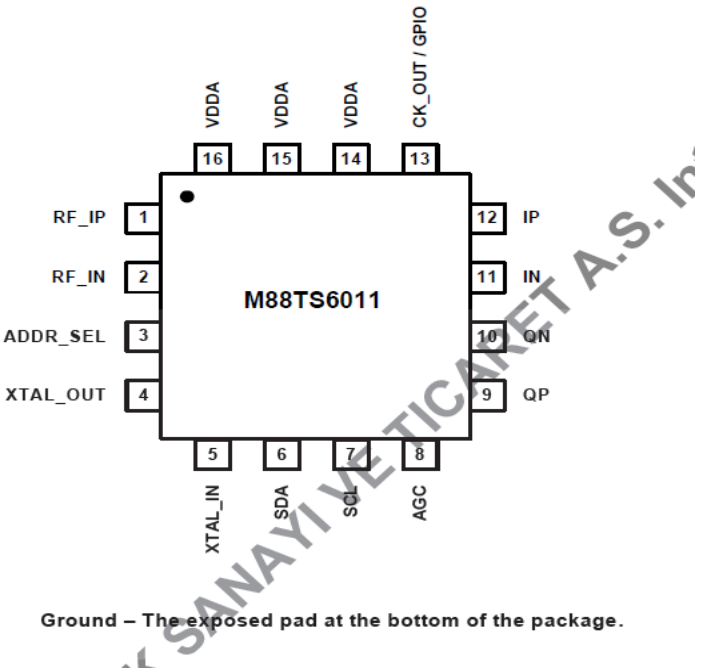
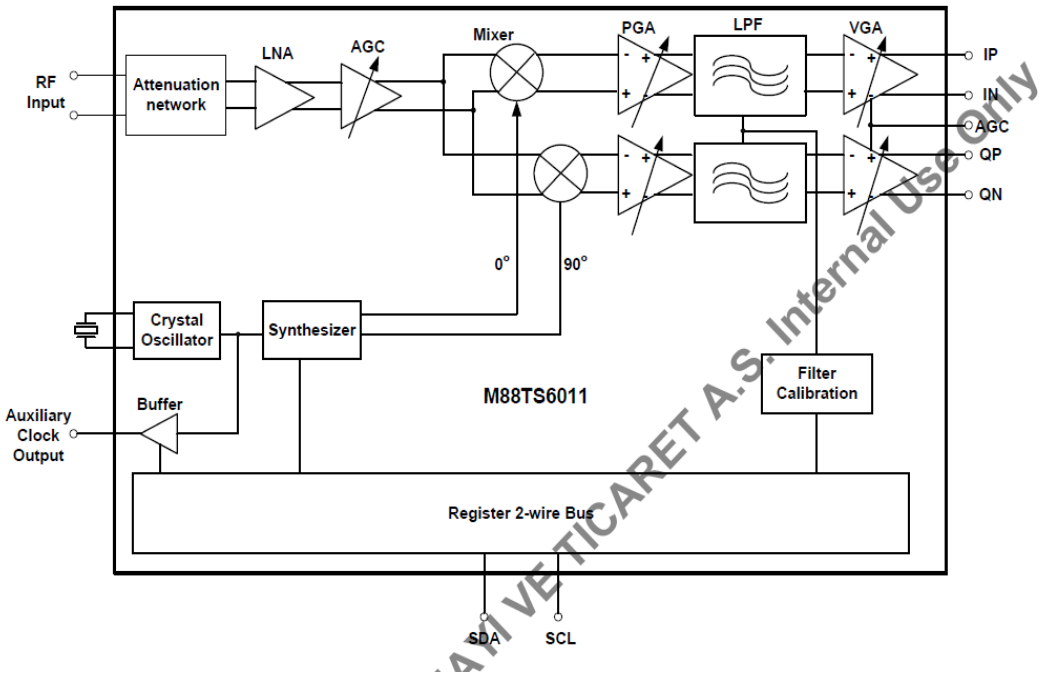


Figure 2: Pin description

Block Diagram



4. AUDIO AMPLIFIER STAGES

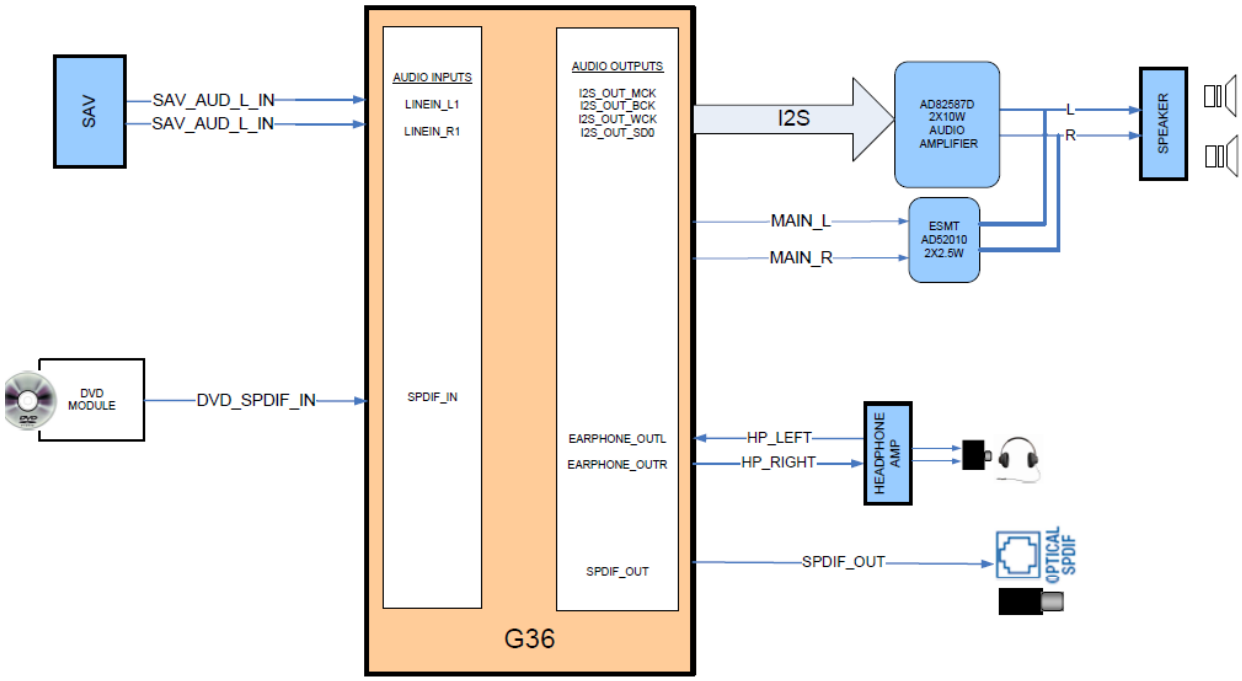


Figure 3: The block diagram of the audio part

A. MAIN AMPLIFIER (U123) (6W/8W/10W OPTIONS)

Description

AD82587D is a digital audio amplifier capable of driving a pair of 8 ohm, 20W or a single 4 ohm, 40W speaker, both which operate with play music at a 24V supply without external heat-sink or fan requirement.

Using I2C digital control interface, the user can control AD82587D's input format selection, DRC (dynamic range control), mute and volume control functions. AD82587D has many built-in protection circuits to safeguard AD82587D from connection errors.

Features

- 16/18/20/24-bit input with I^2S, Left-alignment and Right-alignment data format
- PSNR & DR(A-weighting) Loudspeaker: 97dB (PSNR), 105dB (DR) @ 24V
- Multiple sampling frequencies (Fs)
  - 32kHz / 44.1kHz / 48kHz and
  - 64kHz / 88.2kHz / 96kHz and
  - 128kHz/176.4kHz/192kHz
- System clock = 64x, 128x, 256x, 384x, 512x, 768x,1024x Fs
  - 256x~1024x Fs for 32kHz / 44.1kHz / 48kHz

  - 128x~512x Fs for 64kHz / 88.2kHz / 96kHz
  - 64x~256x Fs for 128kHz /176.4kHz/192kHz

- Supply voltage
  - 3.3V for digital circuit
  - 10V~26V for loudspeaker driver
- Loudspeaker output power for Stereo@ 24V
  - 10W x 2ch into 8_ @ 0.16% THD+N
  - 15W x 2ch into 8_ @ 0.18% THD+N
  - 20W x 2ch into 8_ @ 0.24% THD+N
- Loudspeaker output power for Mono@ 24V
  - 20W x 1ch into 4_ @ 0.17% THD+N
  - 30W x 1ch into 4_ @ 0.2% THD+N
  - 40W x 1ch into 4_ @ 0.24% THD+N
- Sounds processing including:
  - Volume control (+24dB~-103dB, 0.125dB/step)
  - Dynamic range control
  - Power clipping
  - Channel mixing
  - User programmed noise gate with hysteresis window
  - DC-blocking high-pass filter
- Anti-pop design
- Short circuit and over-temperature protection
- I2C control interface with selectable device address
- Internal PLL
- LV Under-voltage shutdown and HV Under-voltage
- detection
- Power saving mode
- Dynamic temperature control

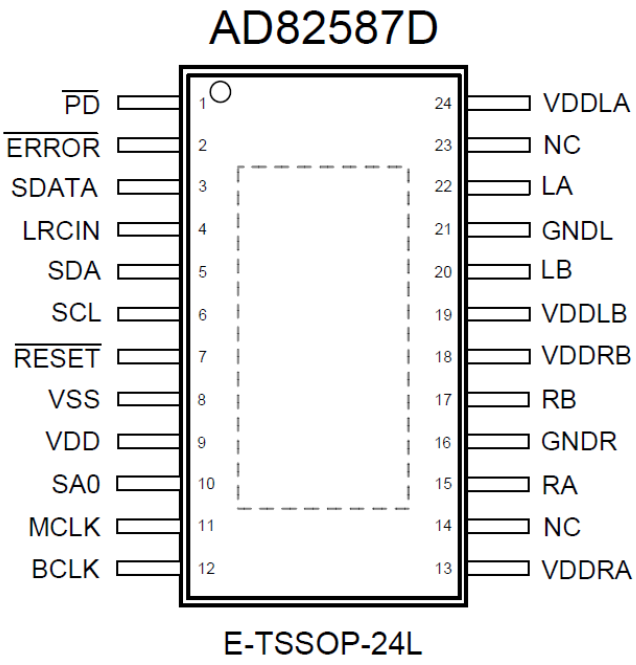


Figure 2: Pin description

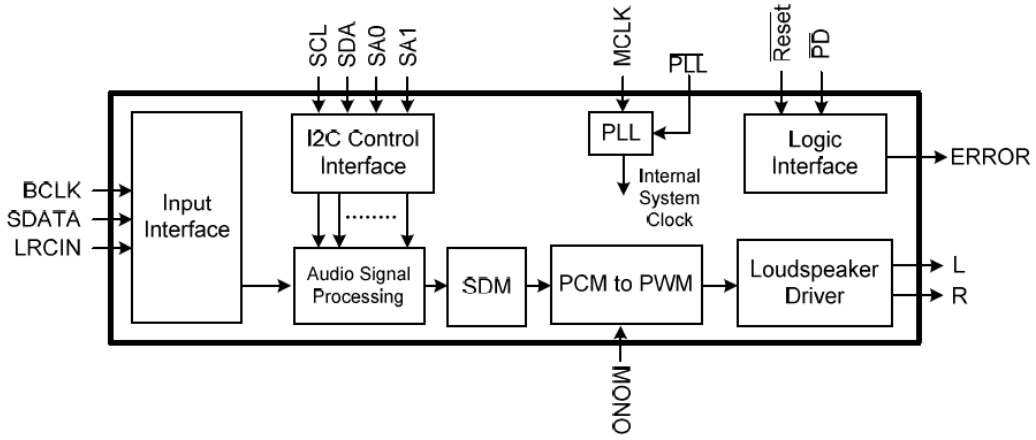


Figure 3: Functional Block Diagram

Symbol	Parameter	Min	Max	Units
DVDD	Supply for Digital Circuit	-0.3	3.6	V
VDDL/R	Supply for Driver Stage	-0.3	30	V
V_i	Input Voltage	-0.3	3.6	V
T_{stg}	Storage Temperature	-65	150	°C
T_J	Junction Operating Temperature	0	150	°C

Table 2: Absolute Maximum Ratings

Symbol	Parameter	Typ	Units
DVDD	Supply for Digital Circuit	3.15~3.45	V
VDDL/R	Supply for Driver Stage	10~26	V
T_J	Junction Operating Temperature	0~125	°C
T_A	Ambient Operating Temperature	0~70	°C

Table 3: Recommended Operating Conditions

B. MAIN AMPLIFIER (U126) (2.5 W OPTION)

Description

The AD52010 is a 3.0W stereo, filter-less class-D audio amplifier. Operating with 5.0V loudspeaker driver supply, it can deliver 3.0W output power into 4 ohm loudspeaker within 10% THD+N or 2.6W at 1% THD+N. The AD52010 is a stereo audio amplifier with high efficiency and suitable for the notebook computer, and portable multimedia device.

Features

- Supply voltage range: 2.5 V to 5.5 V
- Support single-ended or differential analog input
- Low Quiescent Current
- Low Output Noise
- Low shut-down current
- Short power-on transient time
- Internal pull-low resistor on shut-down pins
- Short-circuit protection
- Over-temperature protection
- Loudspeaker power within 10% THD+N
    - 1.78W/ch into 8 ohm loudspeaker
    - >3W/ch into 4 ohm loudspeaker
- Loudspeaker efficiency
    - 93% @ 8 ohm, THD+N=10%
    - 85% @ 4 ohm, THD+N=10%
- E-TSSOP-14L package
- Integrated Feedback Resistor of 300kW

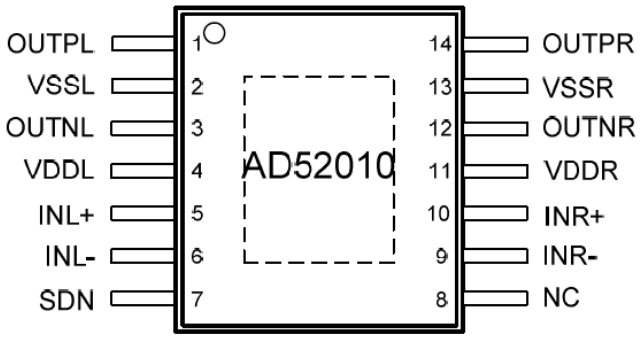


Figure 6: Pin description

NAME	PIN	IO TYPE	DESCRIPTION
	E-TSSOP-14		
OUTPL	1	O	Positive output for left channel.
VSSL	2	G	Power ground for left channel.
OUTNL	3	O	Negative output for left channel.
VDDL	4	P	Power supply for left channel.
INL+	5	I	Positive differential input for left channel.
INL-	6	I	Negative differential input for left channel.
SDN	7	I	Shutdown AD52010 (Low active logic).
NC	8	NC	No internal connected.
INR-	9	I	Negative differential input for right channel.
INR+	10	I	Positive differential input for right channel.
VDDR	11	P	Power supply for right channel.
OUTNR	12	O	Negative output for right channel.
VSSR	13	G	Power ground for right channel.
OUTPR	14	O	Positive output for right channel.
Thermal pad	N/A	G	To connect the package exposed pad to PCB for thermal power dissipation.

Table 4:Pin functions

SYMBOL	PARAMETER	MIN	MAX	UNIT
VDD	Supply for analog cells & loudspeaker driver	2.5	5.5	V
V_{IH}	High-Level Input Voltage	1.3	-	V
V_{IL}	Low-Level Input Voltage	-	0.35	V
T_J	Junction operating temperature	-40	125	℃
Ta	Ambient Operating Temperature	-40	85	℃

Table 5: Recommended operating conditions

C. HEADPHONE AMPLIFIER (U120)

Description

The AD22657B is a 2-Vrms cap-less stereo line driver. The device is ideal for single supply electronics. Cap-less design can eliminate output dc-blocking capacitors for better low frequency response and save cost.

The AD22657B is capable of delivering 2-Vrms output into a 10k ohm load with 3.3V supply. The gain settings can be set by users from 1V/V to 10V/V externally. The AD22657B has under voltage protection to prevent POP noise. Build-in shutdown control and de-pop control sequence also help AD22657B to be a pop-less device.

The AD22657B is available in a 10-pin MSOP package.

Features

- Operation Voltage: 3V to 3.6V
- Cap-less Output
    - Eliminates Output Capacitors
    - Improves Low Frequency Response
    - Reduces POP/Clicks
- Low Noise and THD
    - Typical SNR 107dB
    - Typical Vn 7uVrms
    - Typical THD+N < 0.02%
- Maximum Output Voltage Swing into 2.5k Load
    - 2Vrms at 3.3V Supply Voltage
- Single-ended Input
- External Gain Setting from 1V/V to 10V/V
- Fast Start-up Time: 0.5ms
- Integrated De-Pop Control
- External Under Voltage Protection
- Thermal Protection
- Less External Components Required
- +/-8kV IEC ESD Protection at line outputs

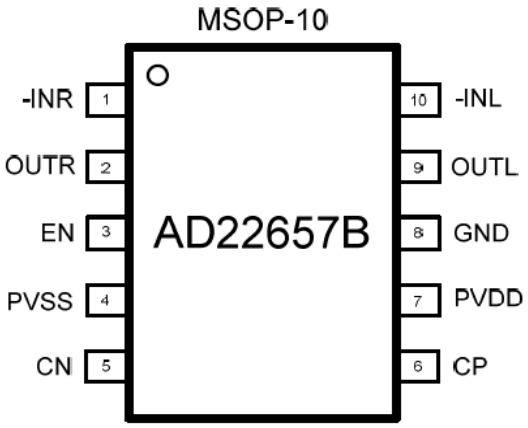


Figure 7: Pin description

No.	Name	Type (1)	Pin Description
1	-INR	I	Right channel OP negative input
2	OUTR	O	Right channel OP output
3	EN	I	Enable input, active high
4	PVSS	P	Supply voltage
5	CN	I/O	Charge-pump flying capacitor negative terminal
6	CP	I/O	Charge-pump flying capacitor positive terminal
7	PVDD	P	Positive supply
8	GND	P	Ground
9	OUTL	O	Left channel OP output
10	-INL	I	Left channel OP negative input

Table 6: Pin function

SYMBOL	PARAMETER		Min	NOM	Max	UNIT
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
V_{IH}	High Level Input Voltage	EN		60		% of V_{DD}
V_{IL}	Low Level Input Voltage	EN		40		% of V_{DD}
T_A	Operating Ambient Temperature Range		-40		85	℃
R_L	Load Resistance		600			Ω

Table 7: Recommended operating conditions

5. POWER STAGE

Figure 8: Power Block Diagram

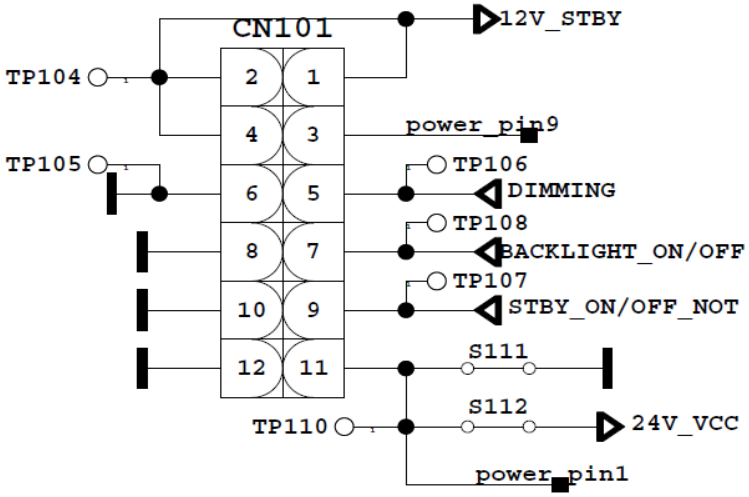


Figure 9: Power Socket and Power Options

Power socket is used for taking voltages which are 24V_VCC, 12V_STBY . These voltages are produced in power card. Also socket is used for giving dimming, backlight and standby signals with power card. Power socket pinning is shown in above figure.

24V_VCC goes directly to the audio part. 12V_STBY is converted several different voltages on the mainboard which are shown in below figure.

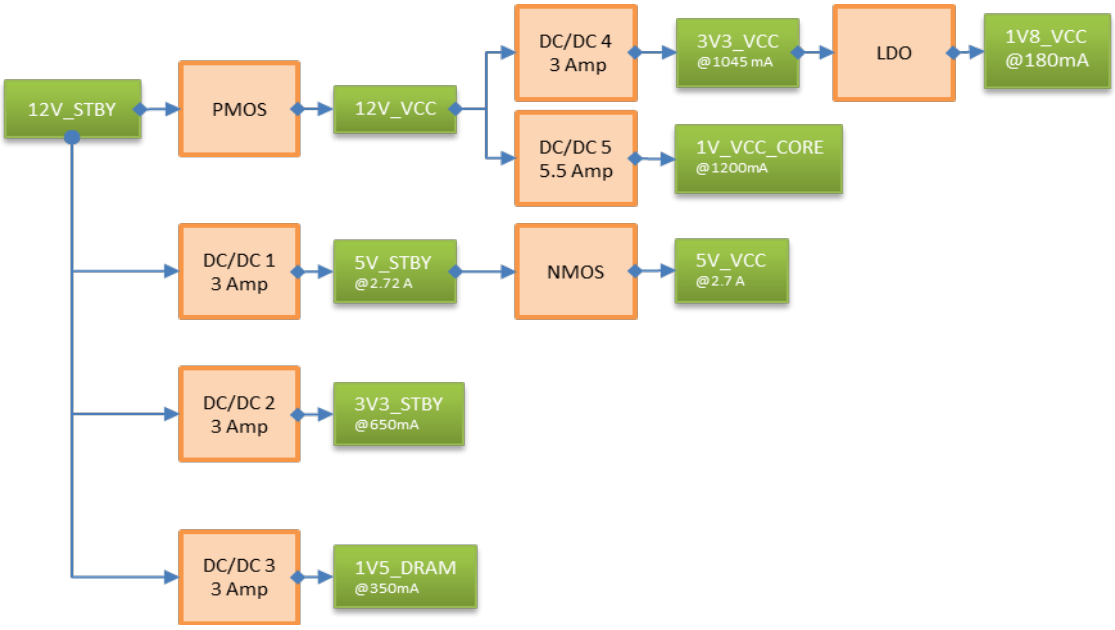


Figure 10: Power Block Diagram

List of the components:

- PMOS(Q105,Q116) → KI5P02DV
- NMOS(Q100) → DMG6402LDM
- DC-DC-1(U101) → RT7278G
- DC-DC-2(U137) → TPS563200-3A
- DC-DC-3(U127) → TPS563200-3A
- DC-DC-4(U100) → TPS563200-3A
- DC-DC-5(U138) → TPS54528
- LDO(U140) → LM1117

A. KI5P02DV (Q105, Q116)

Features

- VDS (V) =-20V
- ID =-4.6 A
- RDS(ON) < 40mΩ (VGS =-4.5V)
- RDS(ON) < 70mΩ (VGS =-2.5V)
- Low Input/Output Leakage

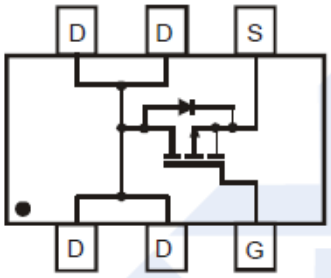


Figure 11: Pin description

■ Electrical Characteristics Ta = 25℃

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{DSS}	I_D=-250μA, V_{GS}=0V	-20			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-20V, V_{GS}=0V			-1	μA
Gate-Body leakage current	I_{GSS}	V_{DS}=0V, V_{GS}=±12V			±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=-250μA	-0.6		-1.2	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=-4.5V, I_D=-4.6A			40	mΩ
		V_{GS}=-2.5V, I_D=-3.8A			70	
On state drain current	$I_{D(ON)}$	V_{GS}=-4.5V, V_{DS}=-5V	-15			A
Forward Transconductance	g_{FS}	V_{DS}=-10V, I_D=-4.6A		9		S
Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=-15V, f=1MHz		820		pF
Output Capacitance	C_{oss}			200		
Reverse Transfer Capacitance	C_{rss}			160		
Gate resistance	R_g	V_{GS}=0V, V_{DS}=0V, f=1MHz		2.5		Ω
Total Gate Charge	Q_g	V_{GS}=-4.5V, V_{DS}=-10V, I_D=-4.5A		10.1		nC
Gate Source Charge	Q_{gs}			1.5		
Gate Drain Charge	Q_{gd}			4.3		
Turn-On DelayTime	$t_{d(on)}$	V_{DS} = -10V, V_{GS} = -4.5V, I_D = -1A, R_G = 6Ω		4.4		ns
Turn-On Rise Time	t_r			9.9		
Turn-Off DelayTime	$t_{d(off)}$			28		
Turn-Off Fall Time	t_f			23.4		
Maximum Body-Diode Continuous Current	I_S				-1.7	A
Diode Forward Voltage	V_{SD}	I_S=-2.1A,V_{GS}=0V	-0.5		-1.4	V

Figure 12: Electrical Characteristic

B. DMG6402LDM (Q100)

Features

- Low RDS(ON)
- Low Input Capacitance
- Fast Switching Speed
- Low Input/Output Leakage

- Lead Free By Design/RoHS Compliant (Note 1)
- Qualified to AEC-Q101 Standards for High Reliability

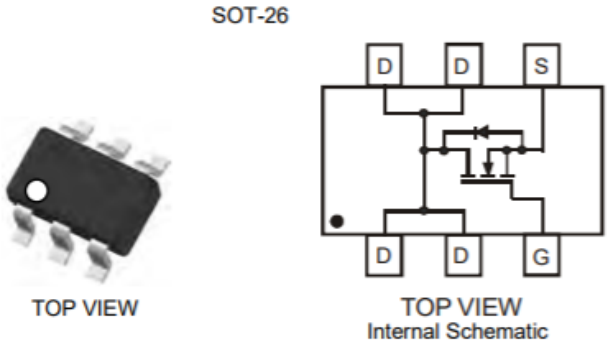


Figure 13: Pin description

Electrical Characteristics @T_A = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 5)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	V_{GS} = 0V, I_D = 250μA
Zero Gate Voltage Drain Current T_J = 25°C	I_{DSS}	-	-	1.0	μA	V_{DS} = 30V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS (Note 5)						
Gate Threshold Voltage	$V_{GS(th)}$	1.0	1.5	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	22 32	27 40	mΩ	V_{GS} = 10V, I_D = 7A V_{GS} = 4.5V, I_D = 5.6A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	10	-	S	V_{DS} = 5V, I_D = 7A
Diode Forward Voltage	V_{SD}	-	0.75	1.0	V	V_{GS} = 0V, I_S = 1A
DYNAMIC CHARACTERISTICS (Note 6)						
Input Capacitance	C_{iss}	-	404	-	pF	V_{DS} =15V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	52	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	45	-	pF	
Gate Resistance	R_g	-	1.51	-	Ω	V_{DS} =0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge	Q_g	-	9.2	-	nC	V_{GS} =10V, V_{DS} = 15V, ID =5.8A
Gate-Source Charge	Q_{gs}	-	1.2	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.8	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	3.41	-	ns	V_{DD} = 15V, V_{GS} = 10V, R_L = 2.6Ω, R_G = 3Ω
Turn-On Rise Time	t_r	-	6.18	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	13.92	-	ns	
Turn-Off Fall Time	t_f	-	2.84	-	ns	

Notes: 5. Short duration pulse test used to minimize self-heating effect.
6. Guaranteed by design. Not subject to production testing.

Thermal Characteristics

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 3)	P_D	1.12	W
Thermal Resistance, Junction to Ambient T_A = 25°C (Note 3)	$R_{\theta JA}$	111	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Notes: 1. No purposefully added lead.
2. Diodes Inc's "Green" policy can be found on our website at http://www.diodes.com/products/lead_free/index.php.
3. Device mounted on FR-4 PCB, with minimum recommended pad layout.
4. Repetitive Rating, pulse width limited by junction temperature.

Table 8: Electrical Characteristics & Maximum ratings

C. RT7278G (U101)

General Description

The RT7278 is a synchronous DC/DC step-down converter with Advanced Constant On-Time (ACOT™) mode control. It achieves high power density to deliver up to 3A output current from a 4.5V to 18V input supply. The proprietary ACOT™ mode offers an optimal transient response over a wide range of loads and all kinds of ceramic capacitors, which allows the device to adopt very low ESR output capacitors for ensuring performance stabilization. In addition, RT7278 keeps an excellent constant switching frequency under line and load variation and the integrated synchronous power switches with the ACOT™ mode operation provides high efficiency in whole output current load range. Cycle-by-cycle current limit provides an accurate protection by a valley detection of low side MOSFET and external soft-start setting eliminates input current surge during startup. Protection functions also include output under voltage protection, output over voltage protection, and thermal shutdown.

Features

- **ACOT™ Mode Enables Fast Transient Response**
- **4.5V to 18V Input Voltage Range**
- **3A Output Current**
- **60mΩ Internal Low Site N-MOSFET**
- **Advanced Constant On-Time Control**
- **Support All Ceramic Capacitors**
- **Up to 95% Efficiency**
- **700kHz Switching Frequency**
- **Adjustable Output Voltage from 0.765V to 8V**
- **Adjustable Soft-Start**
- **Cycle-by-Cycle Current Limit**
- **Input Under Voltage Lockout**
- **Thermal Shutdown**
- **RoHS Compliant and Halogen Free**

Applications

- Industrial and Commercial Low Power Systems
- Computer Peripherals
- LCD Monitors and TVs
- Green Electronics/Appliances
- Point of Load Regulation for High-Performance DSPs, FPGAs, and ASICs

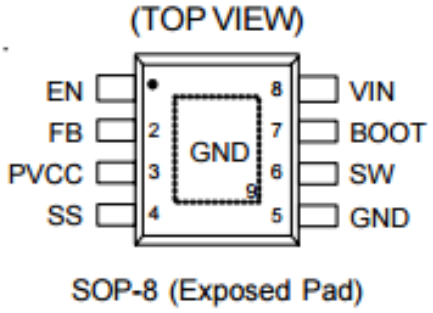


Figure 14: Pin Assignment

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	EN	Enable Control Input. A logic-high enables the converter; a logic-low forces the IC into shutdown mode reducing the supply current to less than 10μA.
2	FB	Feedback Voltage Input. It is used to regulate the output of the converter to a set value via an external resistive voltage divider. The feedback threshold voltage is 0.765V typically.
3	PVCC	Regulator Output for Internal Circuit. Connect a 1μF capacitor to GND to stabilize output voltage.
4	SS	Soft-Start Time Setting. SS controls the soft-start period. Connect a capacitor from SS to GND to set the soft-start period. A 3.9nF capacitor sets the soft-start period of V_{OUT} to 2.6ms.
5, 9 (Exposed Pad)	GND	Ground. The Exposed pad should be soldered to a large PCB and connected to GND for maximum thermal dissipation.
6	SW	Switch Node. Connect this pin to an external L-C filter.
7	BOOT	Bootstrap Supply for High Side Gate Driver. Connect a 0.1μF or greater ceramic capacitor from BOOT to SW pins.
8	VIN	Power Input. The input voltage range is from 4.5V to 18V. Must bypass with a suitably large (≥10μF x 2) ceramic capacitor.

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Current							
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	1.5	10	μA
Quiescent Current		I_Q	V_{EN} = 3V, V_{FB} = 1V	--	0.7	--	mA
Logic Threshold							
EN Input Voltage	Logic-High			2	--	18	V
	Logic-Low			--	--	0.4	
V_{FB} Voltage and Discharge Resistance							
Feedback Threshold Voltage		V_{FB}	4.5V ≤ V_{IN} ≤ 18V	0.757	0.765	0.773	V
Feedback Input Current		I_{FB}	V_{FB} = 0.8V	–0.1	0	0.1	μA
V_{PVCC} Output							
V_{PVCC} Output Voltage		V_{PVCC}	6V ≤ V_{IN} ≤ 18V, 0 < I_{PVCC} < 5mA	4.7	5.1	5.5	V
Line Regulation			6V ≤ V_{IN} ≤ 18V, I_{PVCC} = 5mA	--	--	20	mV
Load Regulation			0 < I_{PVCC} < 5mA	--	--	100	mV
Output Current		I_{PVCC}	V_{IN} = 6V, V_{PVCC} = 4V	--	110	--	mA

Table 9: Functional Pin Description & Electrical Characteristics

D. TPS563200 (U100, U127, U137)

1 Features

- TPS562200 - 2A converter with Integrated 122 mΩ and 72 mΩ FETs
- TPS563200 - 3A converter with Integrated 68 mΩ and 39 mΩ FETs
- D-CAP2™ Mode Control for Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- 650 kHz Switching Frequency
- Advanced Eco-mode™ Pulse-skip
- Low Shutdown Current Less than 10 µA
- 1% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-By-Cycle Overcurrent Limit
- Hiccup-Mode Undervoltage Protection
- Non-latch OVP, UVLO and TSD Protections
- Fixed Soft Start: 1 ms

2 Applications

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

3 Description

The TPS562200 and TPS563200 are simple, easy-to-use, 2 A and 3 A synchronous step-down (buck) converters in 6 pin SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

TPS562200 and TPS563200 operate in Advanced Eco-mode, which maintains high efficiency during light load operation. The devices are available in a 6-pin 1.6mm x 2.9mm SOT (DDC) package, and specified from –40°C to 85°C of ambient temperature.

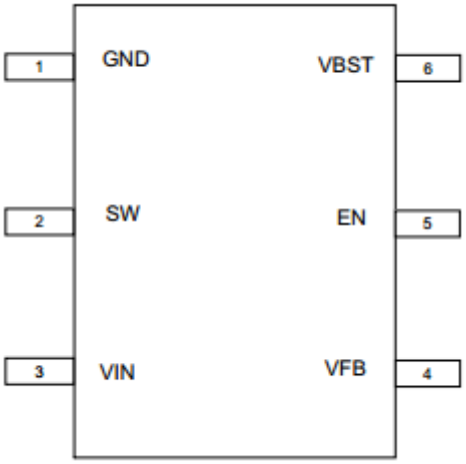


Figure 15: Pin Assignment

Pin Functions

PIN		DESCRIPTION
NAME	NUMBER	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect a 0.1µF capacitor between VBST and SW pins.

Electrical Characteristics

T_J = -40°C to 150°C, VIN = 12V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
$I_{(VIN)}$	Operating – non-switching supply current	V_{IN} current, T_A = 25°C, EN = 5V, V_{FB} = 0.8 V	TPS562200		230	330	µA
			TPS563200		190	290	
$I_{(VINSDN)}$	Shutdown supply current	V_{IN} current, T_A = 25°C, EN = 0 V			3	10	µA
LOGIC THRESHOLD							
$V_{EN(H)}$	EN high-level input voltage	EN		1.6			V
$V_{EN(L)}$	EN low-level input voltage	EN				0.6	V
R_{EN}	EN pin resistance to GND	V_{EN} = 12 V		225	450	900	kΩ
V_{FB} VOLTAGE AND DISCHARGE RESISTANCE							
$V_{FB(TH)}$	V_{FB} threshold voltage	T_A = 25°C, V_O = 1.05 V, I_O = 10mA, Eco-mode™ operation			772		mV
		T_A = 25°C, V_O = 1.05 V, continuous mode operation		758	765	772	mV
$I_{(VFB)}$	V_{FB} input current	V_{FB} = 0.8V, T_A = 25°C			0	±0.1	µA
MOSFET							
$R_{DS(on)h}$	High side switch resistance	T_A = 25°C, V_{BST} – SW = 5.5 V	TPS562200		122		mΩ
			TPS563200		68		mΩ
$R_{DS(on)l}$	Low side switch resistance	T_A = 25°C	TPS562200		72		mΩ
			TPS563200		39		mΩ
CURRENT LIMIT							
I_{ocl}	Current limit (1)	DC current, V_{OUT} = 1.05 V, L_{OUT} = 2.2 µF	TPS562200	2.5	3.2	4.3	A
		DC current, V_{OUT} = 1.05 V, L_{OUT} = 1.5 µF	TPS563200	3.5	4.2	5.3	A
THERMAL SHUTDOWN							
T_{SDN}	Thermal shutdown threshold (1)	Shutdown temperature			155		°C
		Hysteresis			35		
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION							
V_{OVP}	Output OVP threshold	OVP Detect			125% x Vfbth		
V_{UVP}	Output Hiccup threshold	Hiccup detect			65% x Vfbth		
$t_{HiccupOn}$	Hiccup On Time	Relative to soft-start time			1		ms
$t_{HiccupOff}$	Hiccup Off Time	Relative to soft-start time			7		ms
UVLO							
UVLO	UVLO threshold	Wake up VIN voltage		3.45	3.75	4.05	V
		Hysteresis VIN voltage		0.13	0.32	0.55	

(1) Not production tested

Table 10: Functional Pin Description & Electrical Characteristics

E. TPS54528 (U101, U138)

General Description

The TPS54528 is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54528 enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54528 uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light loads. Eco-mode™ allows the TPS54528 to maintain high efficiency during lighter load conditions. The TPS54528 also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

The device operates from 4.5-V to 18-V VIN input. The output voltage can be programmed between 0.76 V and 6 V. The device also features an adjustable soft start time. The TPS54528 is available in the 8-terminal DDA package, and designed to operate from –40°C to 85°C.

Features

- D-CAP2™ Mode Enables Fast Transient Response
- Low Output Ripple and Allows Ceramic Output Capacitor
- Wide VIN Input Voltage Range: 4.5 V to 18 V
- Output Voltage Range: 0.76 V to 6 V
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
    - 65 mΩ (High Side) and 36 mΩ (Low Side)
- High Efficiency, less than 10 µA at shutdown
- High Initial Bandgap Reference Accuracy
- Adjustable Soft Start
- Pre-Biased Soft Start
- 650-kHz Switching Frequency (fSW)
- Cycle By Cycle Over Current Limit
- Auto-Skip Eco-mode™ for High Efficiency at Light Load

Applications

Wide Range of Applications for Low Voltage

- Digital TV Power Supply
- High Definition Blu-ray Disc™ Players
- Networking Home Terminal
- Digital Set Top Box (STB)

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Supply input voltage		4.5	18	V
V_I	Input voltage	VBST	–0.1	24	V
		VBST (10 ns transient)	–0.1	27	
		VBST(vs SW)	–0.1	5.7	
		SS	–0.1	5.7	
		EN	–0.1	18	
		VFB	–0.1	5.5	
		SW	–1.8	18	
		SW (10 ns transient)	–3	21	
		GND	–0.1	0.1	
V_O	Output voltage	VREG5	–0.1	5.7	V
I_O	Output Current	I_{VREG5}	0	5	mA
T_A	Operating free-air temperature		–40	85	°C
T_J	Operating junction temperature		–40	150	°C

Table 11: Recommended operating conditions

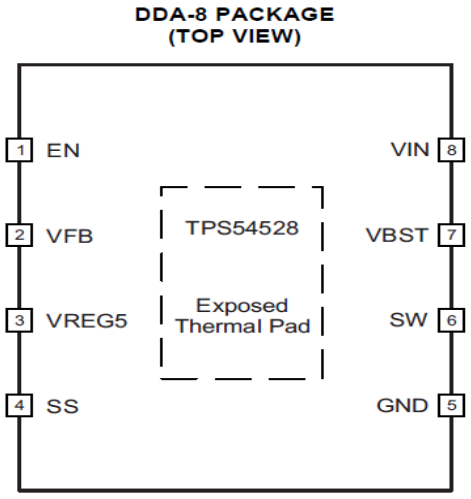


Figure 16: Pin Description

Terminal Functions

TERMINAL		DESCRIPTION
NAME	NO.	
EN	1	Enable input control. EN is active high and must be pulled up to enable the device.
VFB	2	Converter feedback input. Connect to output voltage with feedback resistor divider.
VREG5	3	5.5 V power supply output. A capacitor (typical 1 µF) should be connected to GND. VREG5 is not active when EN is low.
SS	4	Soft-start control. An external capacitor should be connected to GND.
GND	5	Ground terminal. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point.
SW	6	Switch node connection between high-side NFET and low-side NFET.
VBST	7	Supply input for the high-side FET gate drive circuit. Connect 0.1µF capacitor between VBST and SW terminals. An internal diode is connected between VREG5 and VBST.
VIN	8	Input voltage supply terminal.
Exposed Thermal Pad	Back side	Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND.

Table 12: Pin functions

F. LM1117 (U140)

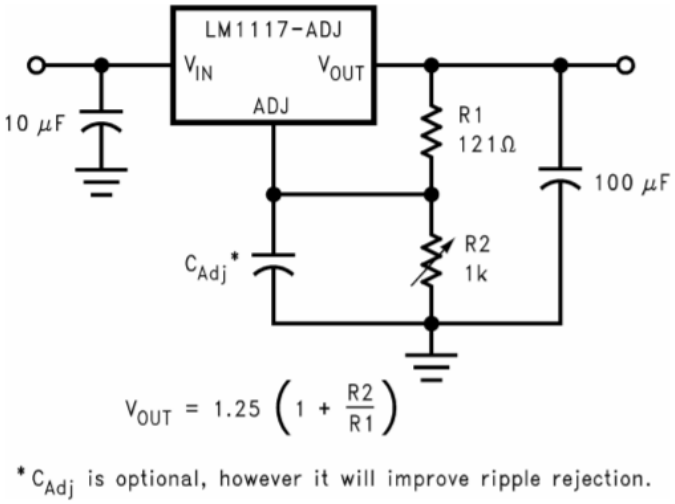
General Description

The LM1117 is a low dropout voltage regulator with a dropout of 1.2 V at 800 mA of load current The LM1117 is available in an adjustable version which can set the output voltage from 1.25 to 13.8 V with only two external resistors. In addition, it is available in five fixed voltages, 1.8 V, 2.5 V, 3.3 V, and 5 V. The LM1117 offers current limiting and thermal shutdown. Its circuit includes a Zener trimmed bandgap reference to assure output voltage accuracy to within ±1%. A minimum of 10-µF tantalum capacitor is required at the output to improve the transient response and stability.

Features

- Available in 1.8 V, 2.5 V, 3.3 V, 5 V, and Adjustable Versions
- Space-Saving SOT-223 and WSON Packages
- Current Limiting and Thermal Protection
- Output Current 800 mA
- Line Regulation 0.2% (Maximum)
- Load Regulation 0.4% (Maximum)
- Temperature Range
    - LM1117: 0°C to 125°C
    - LM1117I: −40°C to 125°C

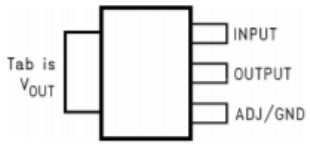
Adjustable Output Regulator



*C_{Adj} is optional, however it will improve ripple rejection.

Pin Configuration and Functions

DCY Package
4-Pin SOT
Top View



Pin Functions

PIN						I/O	DESCRIPTION
NAME	TO-252	WSON	SOT-223	TO-263	TO-220		
ADJ/GND	1	1	1	1	1	—	Adjust pin for adjustable output option. Ground pin for fixed output option.
V_{IN}	3	2, 3, 4	3	3	3	I	Input voltage pin for the regulator
V_{OUT}	2 , TAB	5, 6, 7, TAB	2, 4	2, TAB	2, TAB	O	Output voltage pin for the regulator

Table 13: Functional Pin Description

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Maximum Input Voltage (V_{IN} to GND)			20	V
Power Dissipation(2)		Internally Limited		
Junction Temperature (T_J)(2)			150	°C
Lead Temperature	TO-220 (T) Package, 10 s		260	°C
	SOT-223 (MP) Package, 4 s		260	
Storage Temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage (V_{IN} to GND)			15	V
Junction Temperature (T_J)(1)	LM1117	0	125	°C
	LM1117I	–40	125	

(1) The maximum power dissipation is a function of $T_{J(max)}$, $R_{\theta JA}$, and T_A. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(max)}–T_A)/R_{\theta JA}$. All numbers apply for packages soldered directly into a PCB.

6. MICROCONTROLLER

MEDIATEK G36 (U128)

The MT9288Gxxxxx is MediaTek's latest SOC solution for FHD smart TV. Based on MediaTek's advanced technologies, the MT9288Gxxxxx is integrated with the high-quality video processor which satisfies a variety of customer's requests for image quality to develop the state-of-the-art DTV system. The multi-core CPUs and GPUs deliver high performance for modern Linux and Android TVs. The up-to-date ARM and Mali architecture ensures the best software compatibility.

Applications, such as HTML5, Java, Flash, and so on, are implemented with less efforts.

The MediaTek Professional PQ Engine includes all of MediaTek's most advanced color-tuning tools. MediaTek unique color processor with specially-designed color remapping systems assist System-developers to identify PQ characteristics of all the range of panel models quickly and easily.

The MT9288Gxxxxx for DTV/MM/OTT applications into a single device, reducing the overall system BOM cost. With versatile peripheral connectivity ports, like HDMI, USB, Ethernet, CVBS, etc., the MT9288Gxxxxx can serve as a highquality media center in home entertainment field.

To meet the increasingly popular energy legislative requirements without the use of additional hardware, the MT9288Gxxxxx has an ultra-low power standby mode during which an embedded MCU can act upon standby events and wake up the system as required.

MT9288Gxxxxx is a highly integrated smart TV solution, which supports LVDS output, DTV channel decoding, MPEG decoding, AV1 decoding, and security OS. MT9288Gxxxxx serves full functions of multi-media centers with a high performance CPU, GPU, and AV CODEC/security engines.

1. Combo Front-End Demodulators
2. Advanced Multi-Core CPU and 3D GPU
3. 3D Formatter Engine
4. Multi-Standard A/V Format Decoder
5. MediaTek High Performance Video Processor and MediaTek Professional PQ Engine
6. Home Theater Sound Processor
7. Internet and Variety of Connectivity Support
8. Peripheral and Power Management
9. Robust and Efficient Security Engine
10. Full Multi-Media Decoders Including AV1/ HEVC Decoder Supporting up to FHD/60fps Resolution

High Performance Micro-processor

- ARM Advanced Multi-Core Cortex CPU
- 32KB/32KB I/D cache
- 512KB L2 cache
- Supports Neon instruction sets

3D Graphic GPU

- ARM Advanced Multi-Core Mali GPU
- Vulkan 1.1
- Supports OpenGL ES 3.2/2.0/1.1
- Supports OpenCL 2.0
- Supports DirectX 11 FL9_3
- Supports rendering size up to FHD

Transport Stream De-multiplexer

Supports two parallel and one serial TS inputs interfaces, with or without sync signal

- Supports one of TS PAD is programmable TS
- input/output
- Supports external demodulators
- TS data rate is 140Mbit/s for serial and
- 56MByte/s for parallel
- 128 general purpose PID filters and 128
- section filters for all transport stream demultiplexer
- Supports additional audio/video/PCR filters
- Supports time-shift
- Supports 3DES/DES and AES encryption/decryption
- Supports dual stream decoding for 3D content

MPEG-2 Video Decoder

- ISO/IEC 11172-2 MPEG-1 video format
- decoding
- ISO/IEC 13818-2 MPEG-2 video MP@HL and
- HD level
- Supports resolution up to HDTV (1080p60,
- 1080i, 720p) and SDTV
- Supports dual stream decoding for 3D content

MPEG-4 Video Decoder

- ISO/IEC 14496-2 MPEG-4 ASP video decoding
- up to HD level
- Supports resolutions up to HDTV
- (1080p@60fps)
- Supports Divx Home Theater & HD profiles
- Supports FLV version1 video format decoding

H.264 Decoder

ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding
Supports resolution up to 1920x1080@60fps
Supports bitrate up to 62.5Mbps, the upper limit of level 4.2
Advanced sound processing options available, for example: Dolby1, DTS2, DBX-TV3
Supports digital audio format :
MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC, HE-AAC, WMA, WMA9 Pro
Supports Multi-stream programs :
Dolby MS12-B **Optional**, Dolby MS12-D **Optional**,
Dolby MS12-Y **Optional,** Dolby MS12-Z **Optional**, and
DTS M6 **Optional**, DTS M6 multistream decoder/encoder
Supports Audio Description
Supports MPEG audio encoding
Supports time-shifting PVR
Supports programmable delay for audio/video Synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional
- line-output
- Supports stereo headphone driver

- I2S digital audio output
- S/PDIF digital audio output and input**optional**
- Supports HDMI receiver ARC function
- Supports PDM input for 2/4 channels digital
- Microphone

Analog RGB Compliant Input Ports

- One analog ports support up to 1080P
- Supports PC RGB input up to SXGA@75Hz
- Supports HDTV RGB/YPbPr/YCbCr
- Supports Composite Sync and SOG Sync-on-
- Green
- Automatic color calibration

Analog RGB Auto-Configuration & Detection

- Auto input signal format and mode detection
- Auto-tuning function including phasing,
- positioning, offset and gain configuration
- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

- Three HDMI/DVI input ports
- HDMI 1.4b Compliant
- MediaTek iSwitch for fast HDMI switching
- HDCP 2.2/1.4 Compliant
- Supports HDMI CEC
- Supports HDMI ARC TX
- Robust receiver with excellent long-cable
- Support

MediaTek High Performance Video Processor

- Video Processing Engine
  - − Supports up to 2K FHD@60p
  - − 10/12-bit Internal Data Processing
  - − Arbitrary Frame Rate Conversion
- Video Care Technology
  - − Video Line Broken Artifact Detection and Removal
  - − Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
- Fully Programmable Multi-Function Scaling Engine
  - − High-Quality Filters with Programmable Parameter
  - − An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
  - − Nonlinear Video Scaling supports various modes including Panorama
  - − Supports Dynamic Scaling for RM, VC-1
  - − Fully Programmable Zoom Ratios for Up/Down Scaling
  - − Independent Horizontal and Vertical Zoom
- Deinterlacer
  - −Motion Compensated Video Deinterlacing with Motion Object Stabilizer
  - − Motion Adaptive Deinterlacer
  - − Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
  - − Automatic 3:2/2:2/M:N Pull-Down

  Advanced sound processing options available, for example: Dolby1, DTS2, DBX-TV3
- Supports digital audio format :
  MPEG-1, MPEG-2 (Layer I/II), MP3, AAC-LC,
  HE-AAC, WMA, WMA9 Pro
- Supports Multi-stream programs :
  Dolby MS12-B **Optional**, Dolby MS12-D **Optional**,
  Dolby MS12-Y **Optional,** Dolby MS12-Z **Optional**, and
  DTS M6 **Optional**, DTS M6 multistream decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for audio/video synchronization

Audio Interface

- One L/R audio line-input
- One L/R output for main speaker or additional
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- Supports stereo headphone driver
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- S/PDIF digital audio output and input**optional**
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- Supports PDM input for 2/4 channels digital
- Microphone

Analog RGB Compliant Input Ports

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- Sync Detection for H/V Sync

DVI/HDCP/HDMI Compliant Input Ports

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- Supports HDMI ARC TX
- Robust receiver with excellent long-cable
- Support

− Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
MediaTek Genuine 3D
− Supports Mandatory 3D Format
Backlight Technology
− Supports Direct and Edge Types Local Dimming
− Programmable Light Spread Profile
− Content Adaptive LCD Backlight Control
High Dynamic Range
− Supports SMPTE ST-2084/ST-2086
− Supports ARIB STD-B67(Hybrid Log Gamma)/BT.2100
− Supports 2094-40 (HDR10 plus)
− Supports ITU-R BT.2100
− Full HD Premium Ready
− Dolby Vision
Response Time Compensation
− Supports Overdrive Technology

MediaTek Professional PQ Engine

UltraClear

MediaTek High Performance Video Processor

- Video Processing Engine

− Supports up to 2K FHD@60p
− 10/12-bit Internal Data Processing
− Arbitrary Frame Rate Conversion

- Video Care Technology

− Video Line Broken Artifact Detection and Removal
− Video Detection & Repairing Technology for Lousy Inputs such as Internet Streaming
Fully Programmable Multi-Function Scaling

- Engine

− High-Quality Filters with Programmable Parameter
− An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
− Nonlinear Video Scaling supports various modes including Panorama
− Supports Dynamic Scaling for RM, VC-1
− Fully Programmable Zoom Ratios for Up/Down Scaling
− Independent Horizontal and Vertical Zoom
Deinterlacer
− Motion Compensated Video Deinterlacing with Motion Object Stabilizer
− Motion Adaptive Deinterlacer
− Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal

− MPEG Artifact Removal
 Advanced Adaptive Block Noise Reduction
 Advanced Mosquito Noise Cancellation
− UltraClear Noise Reduction
 3D Motion-Estimation Temporal Filtering
− 3D Noise Reduction
 3D Temporal Noise Reduction for Lousy Air/Cable Input
S-Powers
− Video Enhancement Processor
 Advanced 3D Independent Multi-Band Control Sharpness Technology
 Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
 Advanced Chroma Transient Improvement
 Supports Luma Transient Improvement

− Super Resolution
 Local Detail Enhancement
 SuperiorClear Multi-Directional Anti-Aliasing and Jagged Compensation Technology
 SuperiorClear Enhance Management
MACE
− MediaTek Advanced Color Engine
 MediaTek Graffito Color Manager
 Color Stain Removal Technology
− Standard Color Format and Processing
- Fully Programmable Input/Output
- CSC
- BT601, BT709, BT2020 (CL/NCL)
- xvYCC601, xvYCC709
- AdobeRGB, AdobeYCC601
- sRGB, sYCC601
- Fully Programmable 12-bit RGB
- Gamma

− Gamut Mapping
 Nonlinear/Linear RGB Domain Gamut Mapping
 Supports 2D Gamut Mapping
 Supports 3D Gamut Mapping
Luce
− Contrast Enhancement
 Real-Time Content Adaptive Contrast Enhancement with Chroma Compensated
 Ultra Contrast Dimming
− SDR to HDR

Output Interface

- Single/Dual link 8/10-bit LVDS output
- Supports panel resolution up to Full HD
- 1920x1080@60Hz (LVDS 2ch)
- Supports TCON:miniLVDS 2ch interface, panel resolution up to Full HD@60Hz**optional**
- Supports TCON:EPI interface, panel resolution up to Full HD@60Hz**optional**
- Supports TTL output, update to
- 1920x1080@60Hz
- Supports programmable timing controller
- Supports dithering options
- Spread spectrum output frequency for EMI suppression
- Supports 60Hz 3D polarizd panel (line interleave)
- Supports Cinema output mode

CVBS Video Encoder

- Supports all NTSC/PAL TV Standard
- Stand-alone scaling engine (no vertical scaling up)
- Programmable Hue, Contract, Brightness
- Supports TTX/WSS output

CVBS Video Output

Allows CVBS output of digital content to SCART

2D Graphics Engine

- Hardware Graphics Engine for responsive interactive applications
- Supports line draw, rectangle draw/fill and text draw
- Supports BitBlt, Stretch BitBlt, Italic Bitblt, Mirror BitBlt and Rotate BitBlt
- Supports alpha-blending operation
- Supports source/destination color key and alpha key
- Supports dither
- Supports color format conversion and format
- transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation

VIF Demodulator

- Compliant with NTSC M/N, PAL B, G/H, I, D/K,
- SECAM L/L' standards
- Supports low IF architecture
- Audio/Video internal dual-path processor
- Locking range improvement

ATSC/QAM Demodulator

- ATSC A/53 compliant 8VSB
- ITU-T J.83 Annex B, SCTE DVS-031 compliant
- 64/256QAM receiver
- 2010 - A74 compliant
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel
- interference suppression
- Impulse-Noise suppression

- Integrated deinterleaver RAM for Level 1 J =1 and Level 2 J= 1,2,3.4
- Supports LIF interfaces

ISDB-T DemodulatorOptional

- Compliant with ISDB-T ARIB STD-B31
- Compliant with ISDB-Tsb ARIB STD-B29
- Supports all modes defined in ISDB-T specs
- Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
- Support LIF interfaces
- Impulse-noise suppression
- Phase noise compensation
- Outside-GI performance improvement
- CNR performance improvement

DVB-C Demodulator

- Compliant with ITU J.83 Annex A/C DVB-C (EN
- 300 429)
- Supports 1-7.2 M Baud symbol rate
- Automatic blind channel scan (constellation and symbol rate)
- Supports LIF interfaces
- IIS performance improvement

DVB-T Demodulator

- Compliant with DVB-T (ETSI EN 300 744)
- Nordig 2.2.2, D-book 7.0 compliant
- Accept low IF inputs in 6, 7, 8MHz channel
- bandwidths
- Supports all guard intervals (1/32 to 1/4)
- Supports all constellations (QPSK, 16-QAM,
- 64-QAM)
- Ultra fast automatic blind UHF/VHF channel
- scan
- Optimized for SFN channels with pre/postcursive
- echoes inside/outside the guard
- Phase-Noise suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel
- interference suppression
- CNR performance improvement
- Outside-GI performance improvement
- DVB-T2 Demodulator **Optional**
- Compliant with DVB-T2 (ETSI EN 302 755)
- v1.3.1, T2-base & T2-Lite profile
- Nordig Unified 2.2.2, D-Book 7.0 compliant
- Supports all guard intervals (1/128 to 1/4)
- Supports all FFT modes from 1K to 32K
- Supports all long and short block code rates
- (1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 2/5, 1/3)
- Supports all constellations (QPSK, 16-QAM,
- 64-QAM, 256-QAM)
- Transmit diversity (MISO) support
- Supports all scattered pilot patterns (PP1 to
- PP8)
- Supports rotated and non-rotated
- constellations
- Supports single and multiple PLPs
- Accept low IF inputs in 1.7, 5, 6, 7, 8MHz
- channel bandwidths
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Automatic co-channel and adjacent channel
- interference suppression
- Impulse-Noise suppression
- Outside GI improvement
- Locking time improvement

DVB-S DemodulatorOptional

- Compliant with DVB-S (ETSI EN 300 421)
- Data Rate: 1-70 Msps
- Code Rates: 1/2, 2/3, 3/4, 5/6, 7/8
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and
- carrier frequencies
- Equalizer compensates for channel
- impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel
- interference suppression
- Impulse-Noise suppression

- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking
- and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon
- limit performances
- Integrated signal quality and BER monitors
- Improved CNR performance

DVB-S2 DemodulatorOptional

- Compliant with DVB-S2 (ETSI EN 302 307)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 16APSK, 1-57 Msps for 32APSK
- Constellations: QPSK , 8PSK , 16APSK and 32APSK
  - QPSK Code Rates: 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple
- Transport Streams
- Roll-off factors for pulse shaping: 0.2, 0.25,
- and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and
- carrier frequencies
- Equalizer compensates for channel
- impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel
- interference suppression
- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking
- and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon
- limit performances
- Integrated signal quality and BER monitors

DVB-S2X DemodulatorOptional

- Compliant with DVB-S2 Extensions (ETSI EN 302 307-2, Broadcast services except for Channel Bonding)
- Data Rate: 1-70 Msps for QPSK , 8PSK, 8APSKL, 16APSK, 16APSK-L, 1-57 Msps for 32APSK, and 32APSK-L
- Constellations: QPSK , 8PSK, 8APSK-L, 16APSK, 16APSK-L, 32APSK, and 32APSK-L
  - QPSK Code Rates: 1/4, 1/3, 2/5, 1/2, 3/5, 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 13/45, 9/20, 11/20
  - 8PSK Code Rates: 3/5, 2/3, 3/4, 5/6, 8/9, 9/10, 23/36, 25/36, 13/18
  - 8APSK-L Code Rates: 5/9, 26/45
  - 16APSK Code Rates: 2/3, 3/4, 4/5, 5/6, 8/9, 9/10, 26/45, 3/5, 28/45, 23/36, 25/36, 13/18, 7/9, 77/90
  - 16APSK-L Code Rates: 5/9, 8/15, 1/2, 3/5, 2/3
  - 32APSK Code Rates: 3/4, 4/5, 5/6, 8/9, 9/10, 32/45, 11/15, 7/9
  - 32APSK-L Code Rates: 2/3
- Supports CCM and VCM
- Supports Single Transport Stream and Multiple
- Transport Streams
- Roll-off factors for pulse shaping: 0.05, 0.1,
- 0.15, 0.2, 0.25, and 0.35
- Carrier frequency acquisition range: 5MHz
- Fast automatic blind scan of symbol rates and
- carrier frequencies
- Equalizer compensates for channel
- impairment
- DiSEqCTM 2.0 compatible with LNB controller
- Automatic co-channel and adjacent channel
- interference suppression

- Impulse-Noise suppression
- All digital demodulation and timing recovery
- loops for tracking frequency and clock offset
- Novel carrier recovery algorithms for tracking
- and compensating large phase noises
- Supports Automatic FEC and Modulation
- Integrated FEC decoders for near Shannon
- limit performances
- Integrated signal quality and BER monitors

Connectivity

- Three USB 2.0 host ports
- USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
- Embedded 10/100 Ethernet PHY
- Supports Ethernet Wake-On-Lan

Miscellaneous

- DRAM interface support DDR3
- Supports PVR
- Parallel interface for external parallel eMMC
- flash and NAND flash support
- Power control module with ultra low power
- MCU available in standby mode
- 462-ball BGA package
- Operating Voltages: TBD

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V_{VDD_33}	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V_{VDD_15}	1.43	1.5	1.57	V
Core Supply Voltages	V_{VDD_core}		TBD		V
			TBD		V
CPU Supply Voltages	V_{VDD_cpu}		TBD		V
			TBD		V
Ambient Operating Temperature	T_A	0		70	°C
Junction Temperature	T_J			125	°C

Table 13: Recommended Operating Conditions

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V_{VDD_33}		3.63	V
1.5V Supply Voltages	V_{VDD_15}		1.65	V
Core Supply Voltages	V_{VDD_core}		TBD	V
CPU Supply Voltages	V_{VDD_cpu}		TBD	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.3	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	Tj		150	°C

Table 14: Absolute Maximum Ratings

7. 4 GB EMMC

SAMSUNG EMMC 4GB KLM4G1FETE-B041 (U139)

Description

SAMSUNG eMMC is an embedded MMC solution designed in a BGA package form. eMMC operation is identical to a MMC device and therefore is a sim-ple read and write to memory using MMC protocol v5.1 which is a industry standard. eMMC consists of NAND flash and a MMC controller. 3V supply voltage is required for the NAND area (VDDF or VCC) whereas 1.8V or 3V dual supply voltage (VDD or VCCQ) is supported for the MMC controller. SAMSUNG eMMC supports HS400 in order to improve sequential bandwidth, especially sequential read performance. There are several advantages of using eMMC. It is easy to use as the MMC interface allows easy integration with any microprocessor with MMC host. Any revision or amendment of NAND is invisible to the host as the embedded MMC controller insulates NAND technology from the host. This leads to faster product development as well as faster times to market. The embedded flash management software or FTL(Flash Transition Layer) of eMMC manages Wear Leveling, Bad Block Management and ECC. The FTL supports all features of the Samsung NAND flash and achieves optimal performance.

Key Features

- Embedded MultiMediaCard Ver. 5.1 compatible.
- SAMSUNG eMMC supports features of eMMC5.1 which are defined in JEDEC Standard

- Major Supported Features : HS400, Field Firmware Update, Cache, Command Queuing, Enhanced Strobe Mode, Secure Write Protection, Partition types

- Non-supported Features : Large Sector Size (4KB)

- Backward compatibility with previous MultiMediaCard system specification (1bit data bus, multi-eMMC systems)
- Data bus width : 1bit (Default), 4bit and 8bit
- MMC I/F Clock Frequency : 0 ~ 200MHz
  MMC I/F Boot Frequency : 0 ~ 52MHz
- Temperature : Operation (-25°C ~ 85°C), Storage without operation (-40°C ~ 85°C)

- Power : Interface power →VCCQ(1.70V ~ 1.95V), Memory power → VCC(2.7V ~ 3.6V)

Item	Min	Max	Unit
V_{CCQ}	1.70 (2.7)	1.95 (3.6)	V
V_{CC}	2.7	3.6	V
V_{SS}	-0.5	0.5	V

Table 15: Supply Voltage

8. PMIC STAGE

There are two tconless panel options on the board. With these circuits, 32” LG and 32” BOE tconless panels can be driven. For each panel one of the PMIC circuit is mounted to the board.

A. SW5227C (LG) (U134)

Description

The SW5227C includes a boost & 2-channel buck converter, positive & negative charge pump, isolation FET, GAMMA-6Ch, PVCOM, reset function, level shifter 12ch. The device in a QFN 7X7-56L package is optimized for TFT LCD panel. The boost converter provides the regulated supply voltage for logic voltage for the system (Typical=3.3V). The other buck converter is provided for HALF AVDD power of source driver ICs. A positive and negative charge pump driver provide the adjustable regulated output voltage for VGH and VGL. In addition, this device has an built-in input to output isolation switch that thi makes possible the real isolation. The buck and boost converters operate with a 680kHz, 1.36MHz switching frequency. The level shifter includes 12-channel level shifter with GPM function(6ch) and Non GPM function(6ch). This device has several

device protection function such as under voltage lockout (UVLO), soft-start for buck and boost converter, thermal protection, over current and over voltage protection.

Features

- Current Mode Boost Converter
  - 9V to 15.5V input supply voltage range
  - 12.8V to 19V output voltage range
  - 680 KHz or 1.36 MHz variable switching frequency
  - Type 3.5A output current, 120mΩ N-channel Mosfet
  - External Soft-start
- Voltage Mode Buck Converter1 for TCON
  - 1.6V to 2.0V and 3.0V to 3.6V output voltage range (Typical=3.3V)
  - 680 KHz or 1.36 MHz variable switching frequency
  - Type 2A output current, 200mΩ Mosfet
  - Built in 500us soft-start
- Voltage Mode Buck Converter3 for Half VDD
  - 6.4V to 9.5V output voltage range
  - 1.36 MHz fix switching frequency
  - Type 1.3A output current, 300mΩ Mosfet
  - Soft-start tracking with boosts converter
- Regulated Positive and Negative Charge Pump Driver
- Built-in Isolated FET
- GAMMA Buffer 6Ch
- PVCOM Controller and High Performance Op-Amplifier
- 56-Pin, 7mm x 7mm. QFN Package

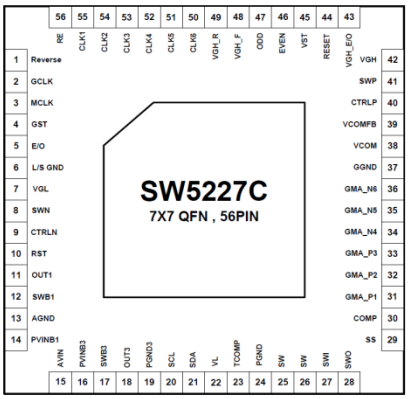


Figure 17: Pin Description

B. ANX6861 (BOE) (U131)

Description

The ANX6861 is an integrated power supply solution optimized for large thin-film transistor (TFT) liquid crystal display (LCD) TV panels which generates all voltage rails for the TFT LCD bias (AVDD, VGH, VGL,VCOM) and also a buck regulator for system logic supply. It is especially designed for 12V input. For better display quality control, the device also provides Gate-Pulse-Modulation block and high accuracy Gamma voltage reference for driver IC.

The boost regulator provides TFT source driver AVDD voltage. The integrated N-channel FET operates at a fixed frequency of 500k/750kHz which has a current limit up to 3.5A and can support output voltages up to 20V.

The buck regulator supplies system logic power with a current limit of 3.2A. It includes an internal power Mosfet and fixed frequency operation allowing the use of small inductors and feasure internal soft-start function to limit inrush current and use current mode control to perform fast load transient response. The buck regulator is compensated by an external RC network.

The gate-on and gate-off charge pumps provide TFT-LCD gate drivers regulated gate-on and gate-off supplies. Both outputs can be adjusted by external resistive voltage dividers. Internal soft-start function is also included.

The integrated operational amplifier is typically used for LCD VCOM driving. It features fast slew rate, wide bandwidth, and rail-to-rail output which can sink or source up to 200mA.

The GPM is a flicker compensation circuit to reduce the coupling effect of gate lines; the gate-shaping timing is controlled by the timing-controller to modulate the Gate-on voltage VGHM.

The high voltage Gamma reference ensures a stable voltage to generate the Gamma correction voltage. The ANX6861 is available in a thin 48-pin 7x7mm WQFN green package.

Features

- 8V to 16.5V input supply
- Current-mode boost regulator
    - 500k/750kHz selectable frequency
    - Integrated 20V/3.5A 100mΩ FET
    - Fast transient response to pulsed load
    - High frequency up to 90%
    - Adjustable soft-start
    - Adjustable current limit for over current protection
    - Adjustable high-accuracy output voltage
    - Over voltage protection
- Current mode buck regulator
    - Integrated 20V/3.2A 100mΩ FET
    - Fast transient response
    - Internal compensation
    - High efficiency
    - Internal 3ms soft-start
    - Adjustable high-accuracy output voltage

- VGH positive charge pump controller
- VGL negative charge pump controller
- High voltage LDO for gamma reference
    - Adjustable high accuracy output voltage
    - Low drop-out voltage at 60mA output current (0.25V)
- Integrated high performance operational amplifier
    - ±200mA output short circuit current
    - -45V/us fast slew rate
- Reset Function
- GPM Controller
    - Adjustable falling time
    - Adjustable turn-on delay
- External gate control for AVDD sequencing
- Thermal shutdown
- Thin 7x7 mm 48-lead WQFN package

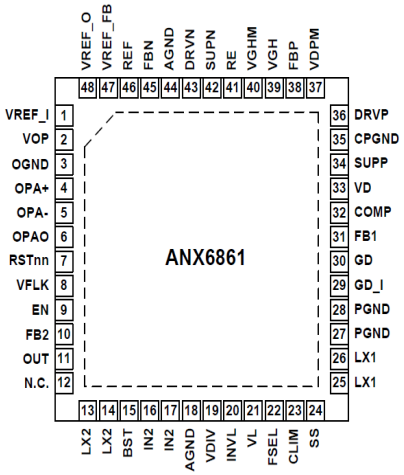
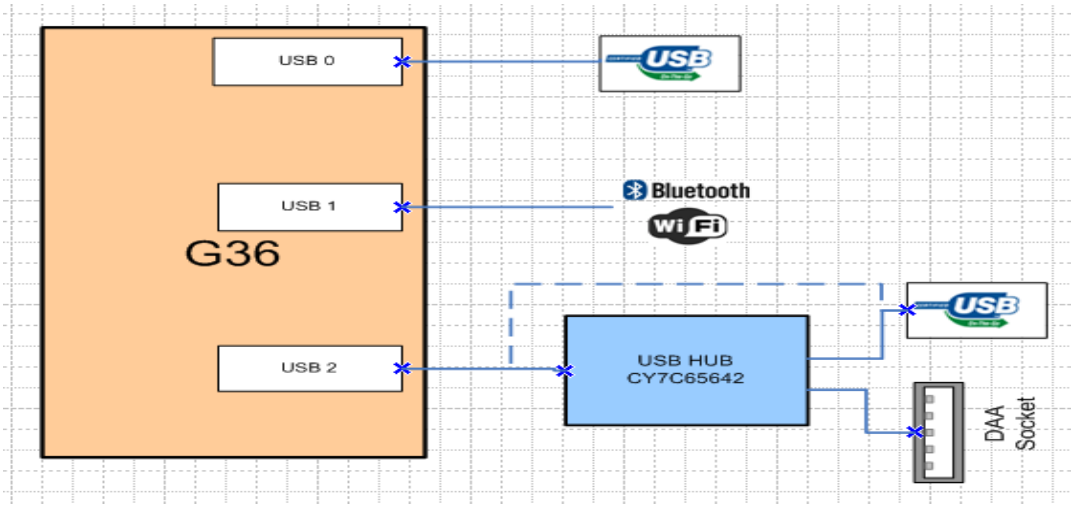


Figure 18: Pin description

9. USB INTERFACE



A. USB POWER SWITCH TPS2553-1 (U109-U117-U122)

FEATURES

- **Up to 1.5 A Maximum Load Current**
- **±6% Current-Limit Accuracy at 1.7 A (typ)**
- **Meets USB Current-Limiting Requirements**
- **Backwards Compatible with TPS2550/51**
- **Adjustable Current Limit, 75 mA–1300 mA (typ)**
- **Constant-Current (TPS2552/53) and Latch-off (TPS2552-1/53-1) Versions**
- **Fast Overcurrent Response - 2-µs (typ)**
- **85-mΩ High-Side MOSFET (DBV Package)**
- **Reverse Input-Output Voltage Protection**
- **Operating Range: 2.5 V to 6.5 V**
- **Built-in Soft-Start**
- **15 kV ESD Protection per IEC 61000-4-2 (with External Capacitance)**
- **UL Listed – File No. E169910 and NEMKO IEC60950-1-am1 ed2.0**

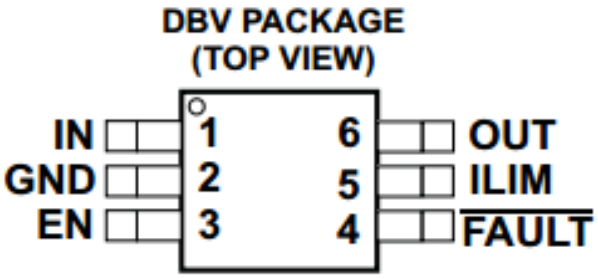
APPLICATIONS

- **USB Ports/Hubs**
- **Digital TV**
- **Set-Top Boxes**
- **VOIP Phones**

DESCRIPTION

The TPS2552/53 and TPS2552-1/53-1 power-distribution switches are intended for applications where precision current limiting is required or heavy capacitive loads and short circuits are encountered and provide up to 1.5 A of continuous load current. These devices offer a programmable current-limit threshold between 75 mA and 1.7 A (typ) via an external resistor. Current-limit accuracy as tight as ±6% can be achieved at the higher current-limit settings. The power-switch rise and fall times are controlled to minimize current surges during turn on/off.

TPS2552/53 devices limit the output current to a safe level by using a constant-current mode when the output load exceeds the current-limit threshold. TPS2552-1/53-1 devices provide circuit breaker functionality by latching off the power switch during overcurrent or reverse-voltage situations. An internal reverse- voltage comparator disables the power-switch when the output voltage is driven higher than the input to protect devices on the input side of the switch. The $\overline{\text{FAULT}}$ output asserts low during overcurrent and reverse-voltage conditions.



EN = Active High for the TPS2553

B. HX2VL VERY LOW POWER USB 2.0 TETRAHUB CONTROLLER (U129)

Description

HX2VL is Cypress's next generation family of high- performance,very low-power USB 2.0 hub controllers. HX2VL has integrated upstream and downstream transceivers; a USB serial interface engine (SIE); USB hub control and repeater logic; and transaction translator (TT) logic. Cypress has also integrated external components such as voltage regulator and
pull-up/pull-down resistors, reducing the overall BOM required to implement a USB hub system.

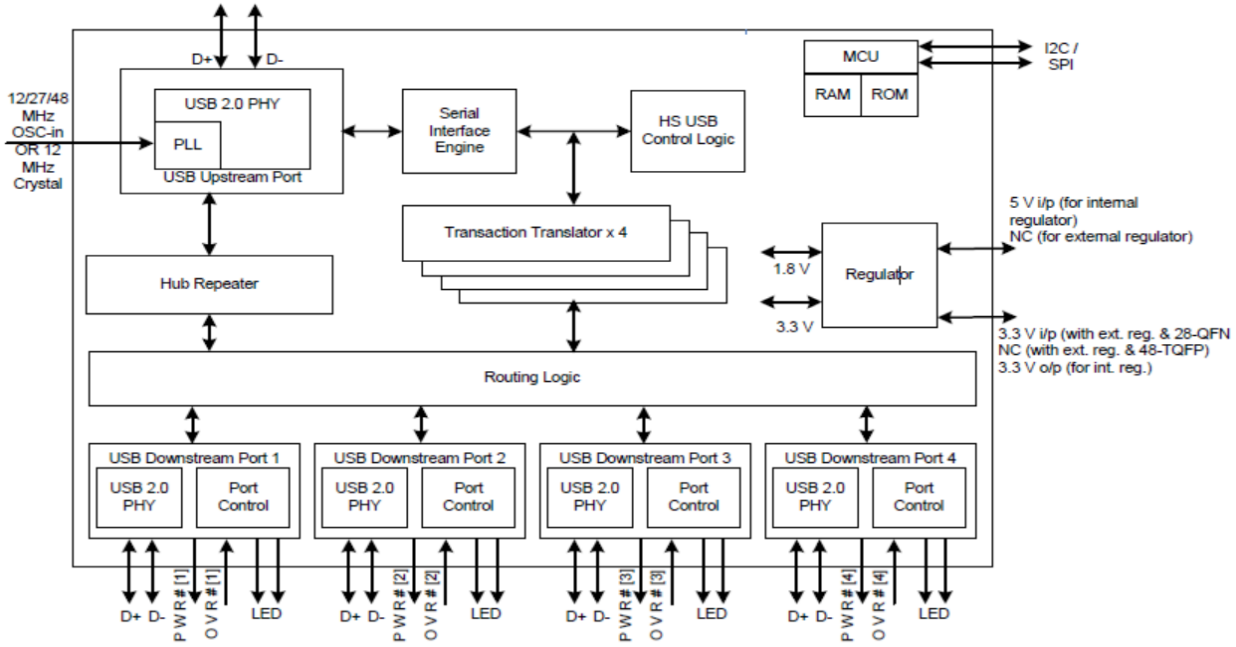
The CY7C65642 is a part of the HX2VL portfolio with four downstream ports and and independent TT dedicated for each downstream port. This device option is for low-power but
high-performance applications that require up to four downstream ports. The CY7C65642 is available in 48-pin TQFP and 28-pin QFN package options.

Features

- High-performance, low-power USB 2.0 hub, optimized for low-cost designs with minimum bill-of-material (BOM).
- USB 2.0 hub controller
    - Compliant with USB2.0 specification
    - Up to four downstream ports support
    - Downstream ports are backward compatible with FS, LS
    - Multiple translator (TT), one per downstream port for maximum performance.
- Very low-power consumption
    - Supports bus-powered and self-powered modes
    - Auto switching between bus-powered and self-powered
    - Single MCU with 2 K ROM and 64 byte RAM
    - Lowest power consumption.

- Highly integrated solution for reduced BOM cost
    - Internal regulator – single power supply 5 V required.
    - Provision of connecting 3.3 V with external regulator.
    - Integrated upstream pull-up resistor
    - Integrated pull-down resistors for all downstream ports
    - Integrated upstream/downstream termination resistors
    - Integrated port status indicator control
    - 12-MHz +/-500 ppm external crystal with drive level 600 uW (integrated PLL) clock input with optional 27/48-MHz oscillator clock input.
    - Internal power failure detection for ESD recovery
- Downstream port management
    - Support individual and ganged mode power management
    - Overcurrent detection
    - Two status indicators per downstream port
    - Slew rate control for EMI management
- Maximum configurability
    - VID and PID are configurable through external EEPROM
    - Number of ports, removable/non-removable ports are configurable through EEPROM and I/O pin configuration
    - I/O pins can configure gang/individual mode power switching, reference clock source and polarity of power switch enable pin
    - Configuration options also available through mask ROM
- Available in space saving 48-pin TQFP (7 × 7 mm) and 28-pin QFN (5 × 5 mm) packages Supports 0 ◦C to +70 ◦C temperature range

Block Diagram



10. CI INTERFACE

17MB181TC Digital CI Interface Block diagram:

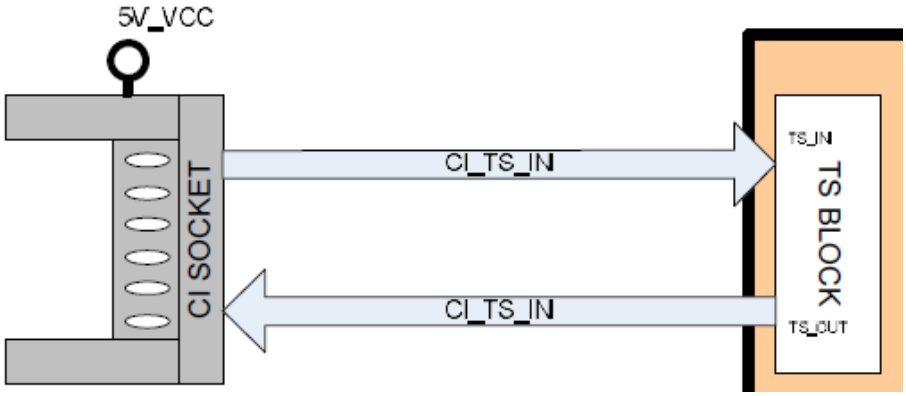


Figure 19: CI interface

11. SOFTWARE UPDATE

MAIN SOFTWARE UPDATE

In MB181TC project, please follow software update procedure:

1. 02_rom_emmc_boot_mb181.bin, mb181_en.bin, usb_auto_update_G36.txt and mboot_emmc_mb181.bin documents should be copied directly inside root of a flash memory (not in a folder).
2. Insert flash memory to the TV when TV is powered off.

3. While pushing the OK button on remote control, then power on and wait. TV will power-up itself.
4. If First Time Installation screen comes, it means software update procedure is successful.

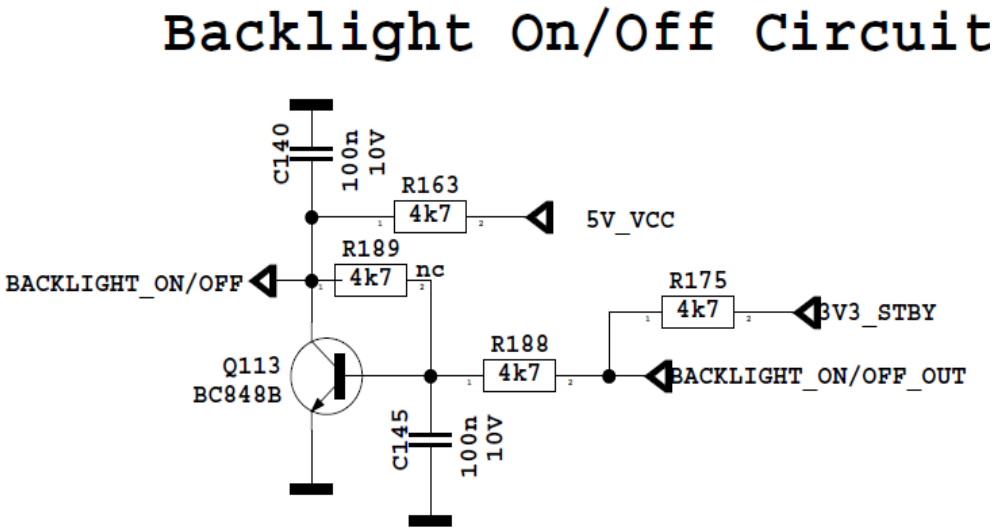
12. TROUBLESHOOTING

A. NO BACKLIGHT PROBLEM

Problem: If TV is working, led is normal and there is no picture and backlight on the panel.

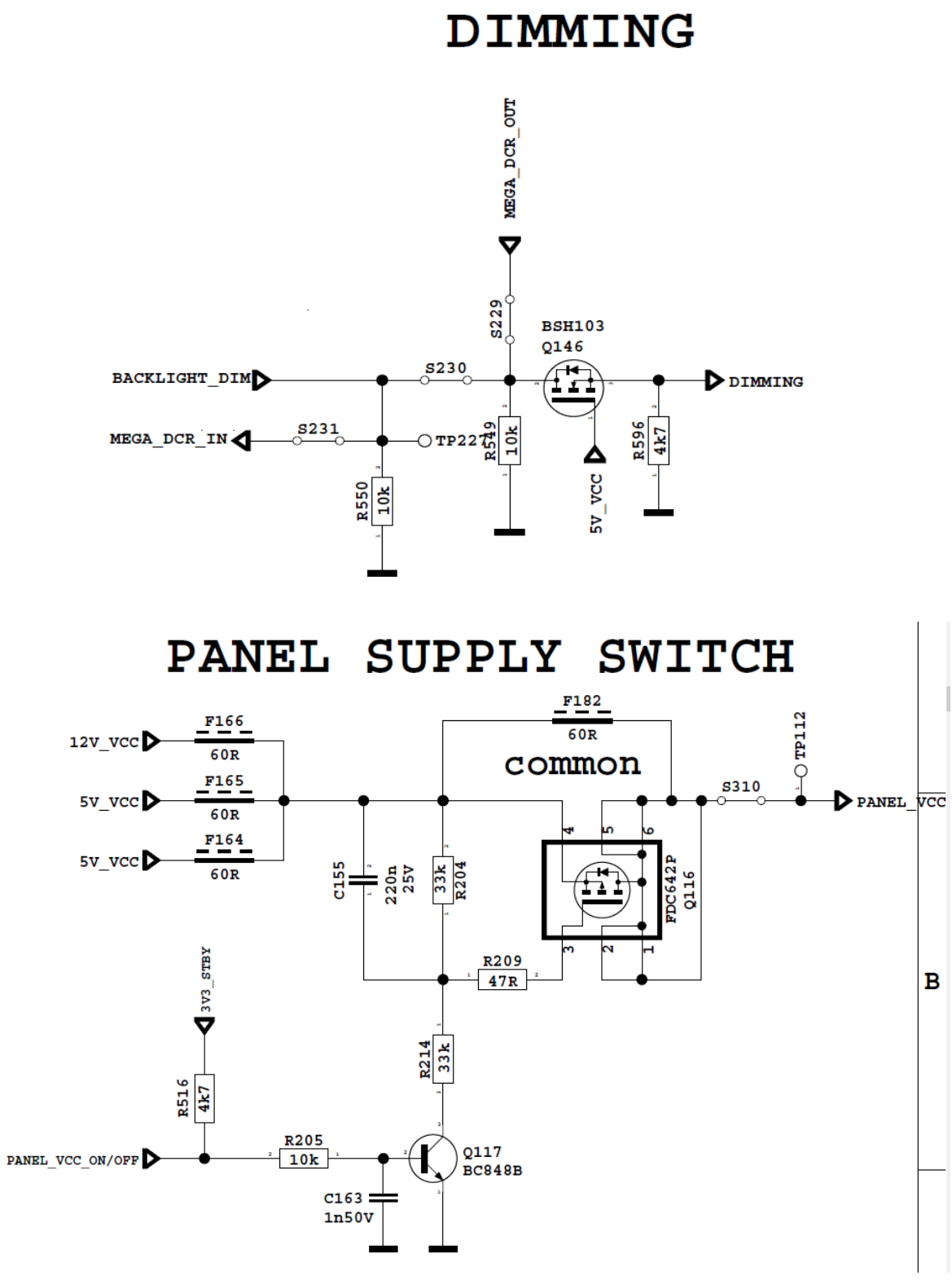
Possible causes: Backlight pin, dimming pin, backlight supply, stby on/off pin

BACKLIGHT_ON/OFF pin should be high when the backlight is ON. Collector pin of Q113 must be low when the backlight is OFF. If it is a problem, please check Q106. Also it can be tested in TP108 in main board. Please also check panel cables.

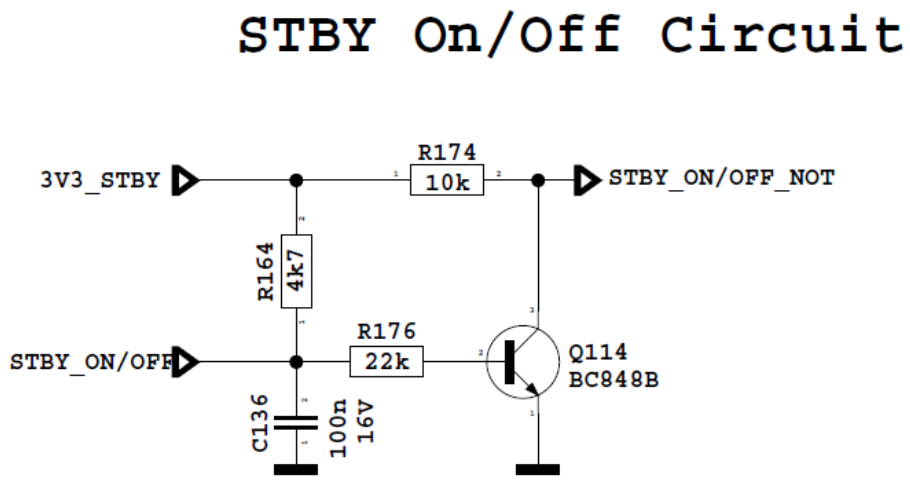


Dimming pin should be high or square wave in open position. It also can be checked at TP106. Please also check panel or power cables and connectors.

Backlight power supply should be in panel specs. Please check Q116, shown below; also it can be checked TP112.



STBY_ON/OFF_NOT should be low for TV on condition, please check Q114's collector.

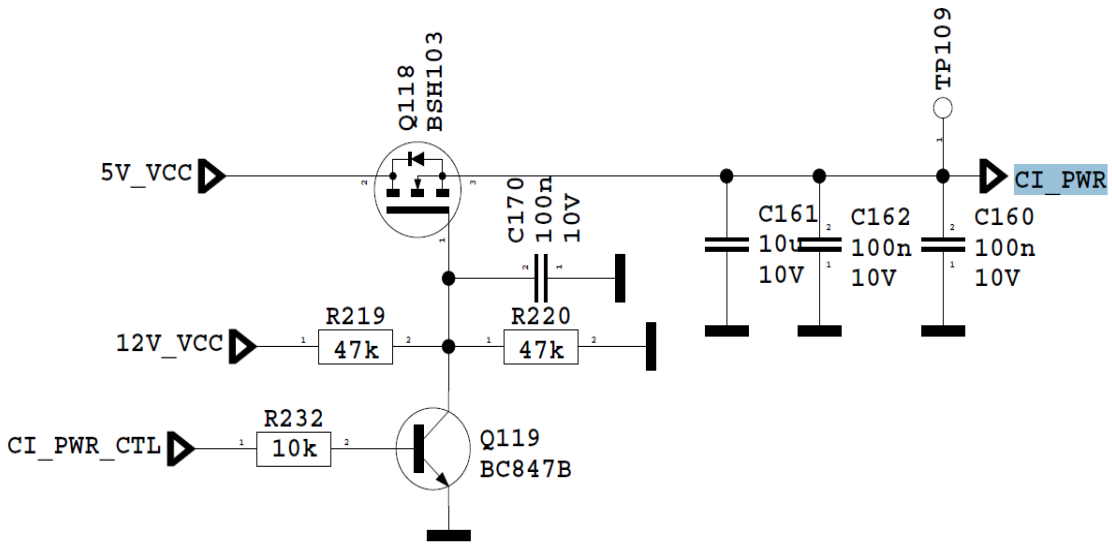


B. CI MODULE PROBLEM

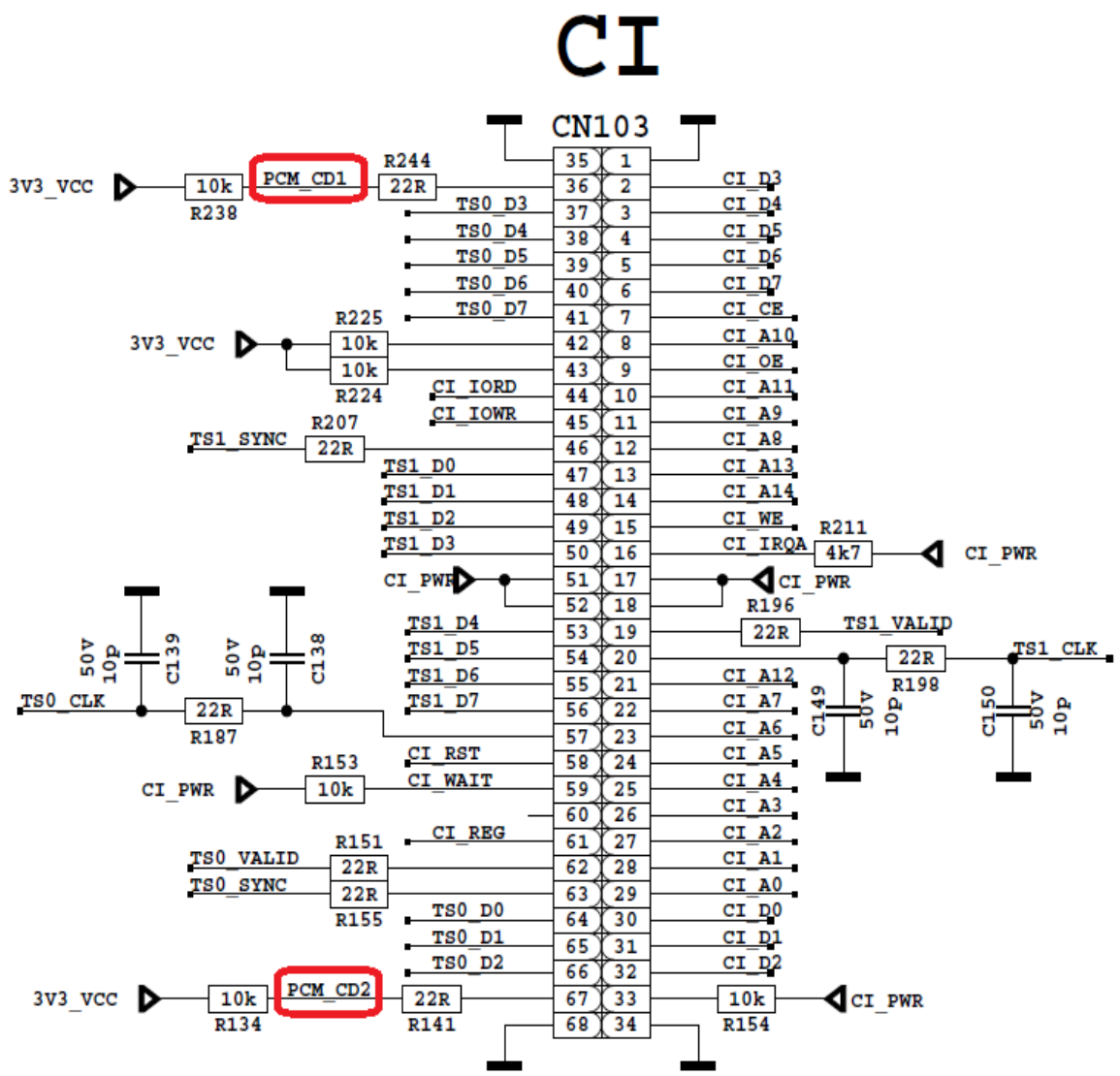
Problem: CI is not working when CI module inserted.

Possible causes: Supply, suply control pin, detects pins, mechanical positions of pins.

- CI supply should be 5V when CI module inserted. If it is not 5V please check CI_PWR_CTRL, this pin should be low.



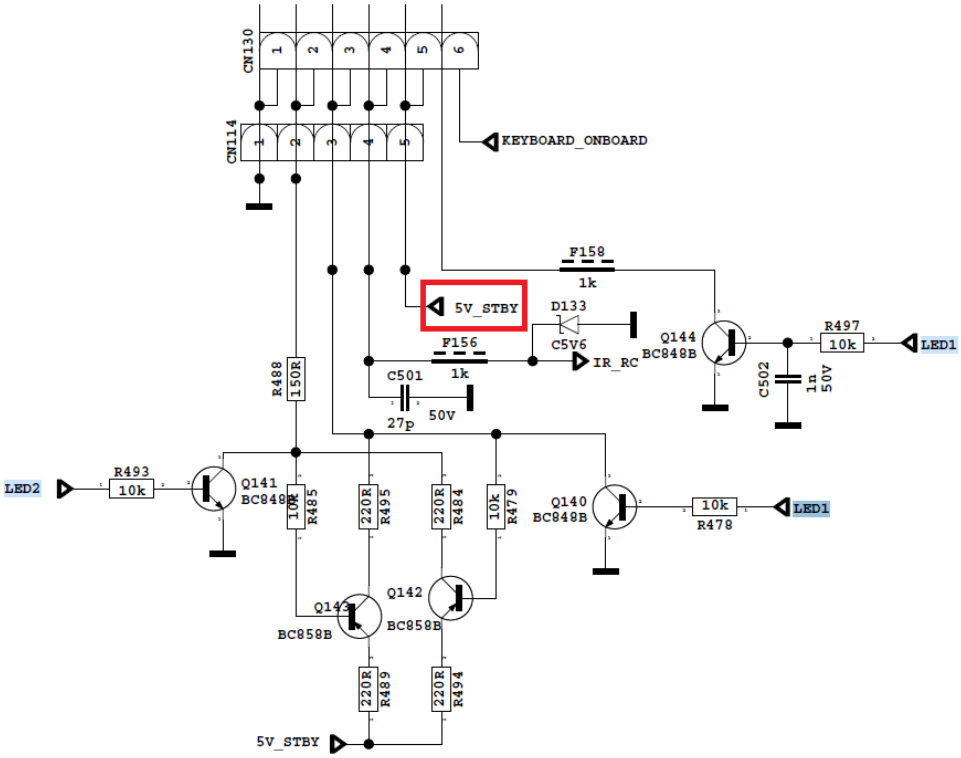
- Please check mechanical position of CI module. Is it inserted properly or not?
- Detect ports should be low. If it is not low please check CI connector pins, CI module pins.



C. IR PROBLEM

Problem: LED or IR not working

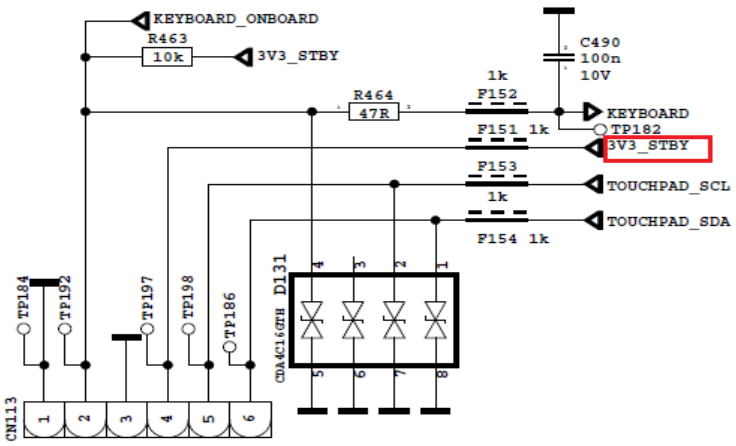
Check LED card supply on MB181TC chasis.



D. KEYPAD TOUCHPAD PROBLEMS

Problem: Keypad or Touchpad is not working

Check keypad supply on MB181TC.



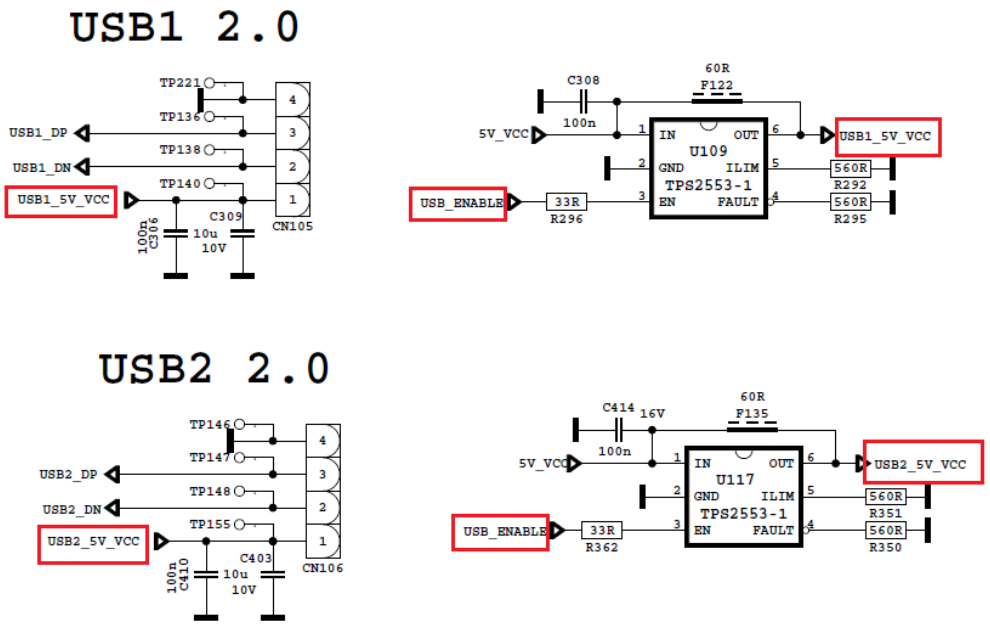
KEYBOARD

E. USB PROBLEMS

Problem: USB is not working or no USB Detection.

Check USB Supply, It should be nearly 5V. Also USB Enable should be logic high.

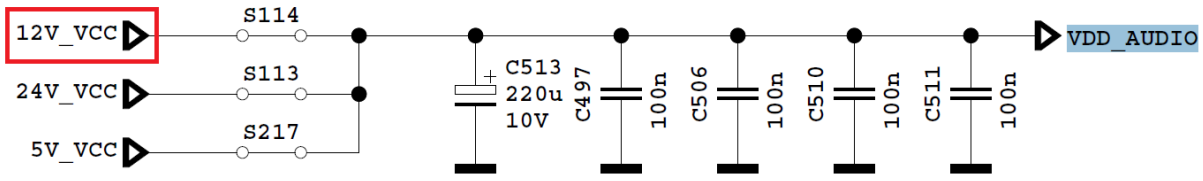
USB Control is optional, so U109 and U117 may not be added. Check supply voltages only.

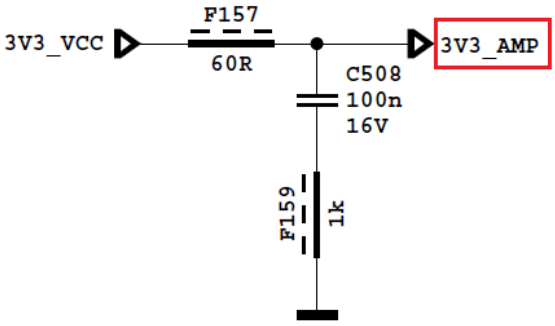


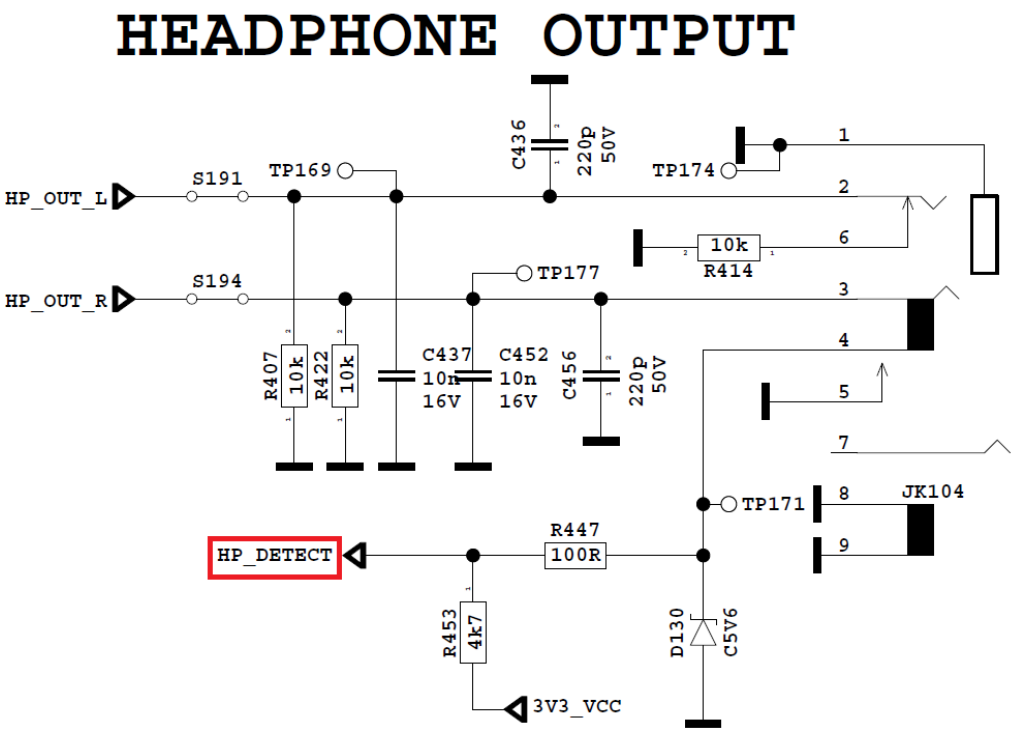
F. NO SOUND PROBLEM

Problem: No audio at main TV speaker outputs.

Check supply voltages of 12V_VCC, VDD_AUDIO and 3V3_AMP with a voltage-meter. There may be a problem in headphone connector or headphone detect circuit. Measure voltage at HP_DETECT pin, it should be 3.3v.







G. STANDBY ON/OFF PROBLEM

Problem: Device cannot boot, TV hangs in standby mode.

There may be a problem about power supply. Check main supplies with a voltage-meter. Also there may be a problem about SW. Try to update TV with latest SW. Additionally it is good to check SW printouts via Teraterm program. These printouts may give a clue about the problem. You can use VGA for Teraterm program connection.

H. NO SIGNAL PROBLEM

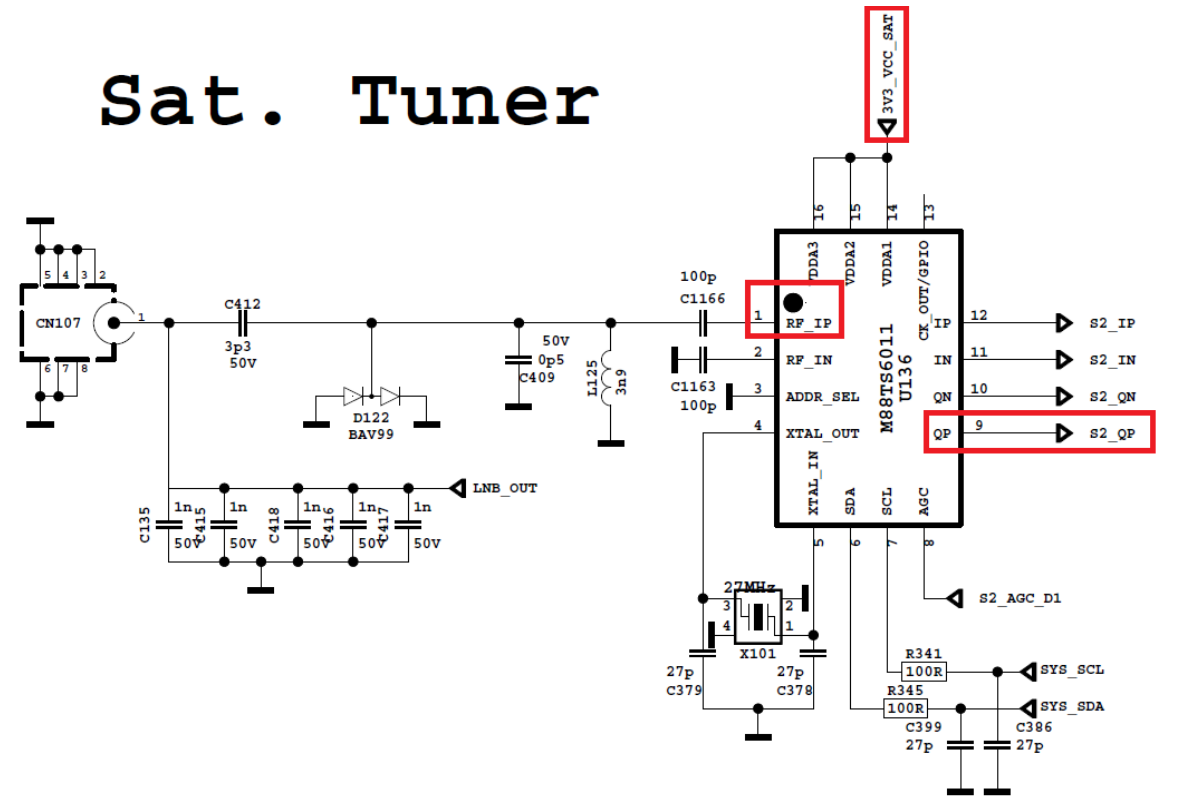
Problem: No signal or Low signal in DVB-S/S2 mode.

Check signal cables and LNB voltage, if there is no problem, check M88TS6011 (U136) supply voltages; 3V3_VCC_SAT.

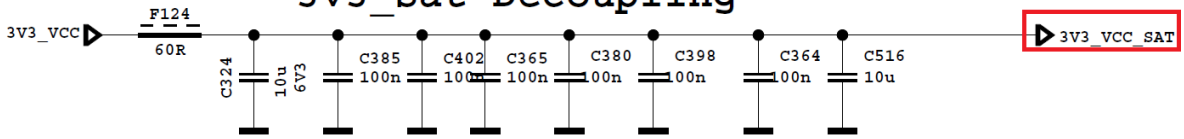
If the above measurements are OK, then measure the voltage from the PIN1 of U136.

If the PIN9 voltage is equal to 0V, please check i2c waveforms and software. If the PIN9 voltage is lower than 1V(e.g: 0.8Vor 0.3V), change the U136 with a new part.

Sat. Tuner



3v3_Sat Decoupling

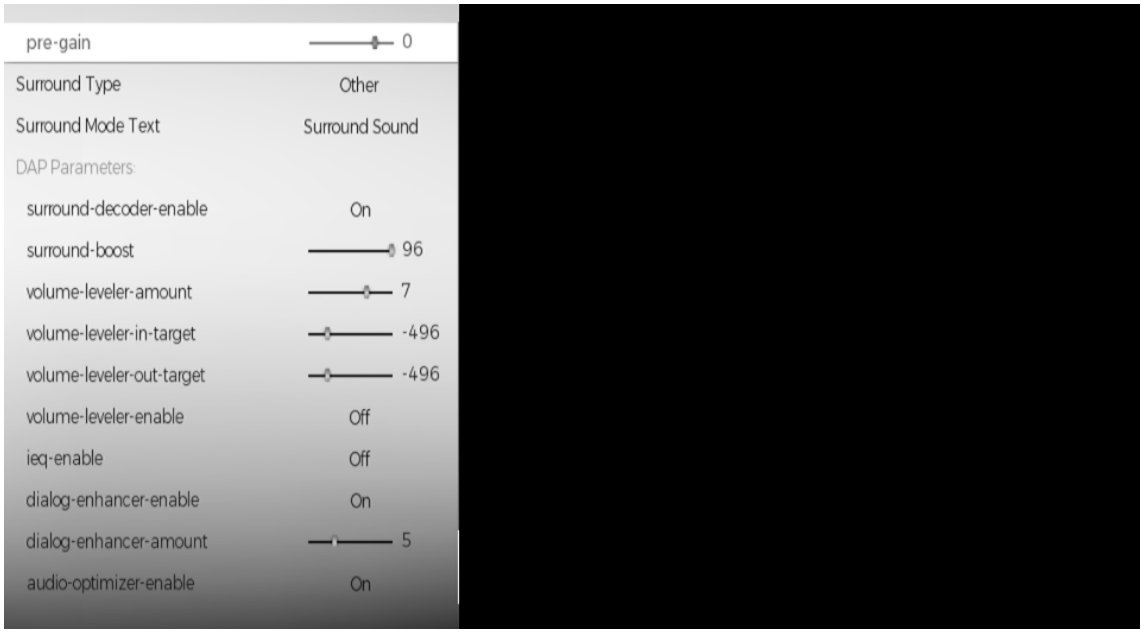


13. SERVICE MENU SETTINGS

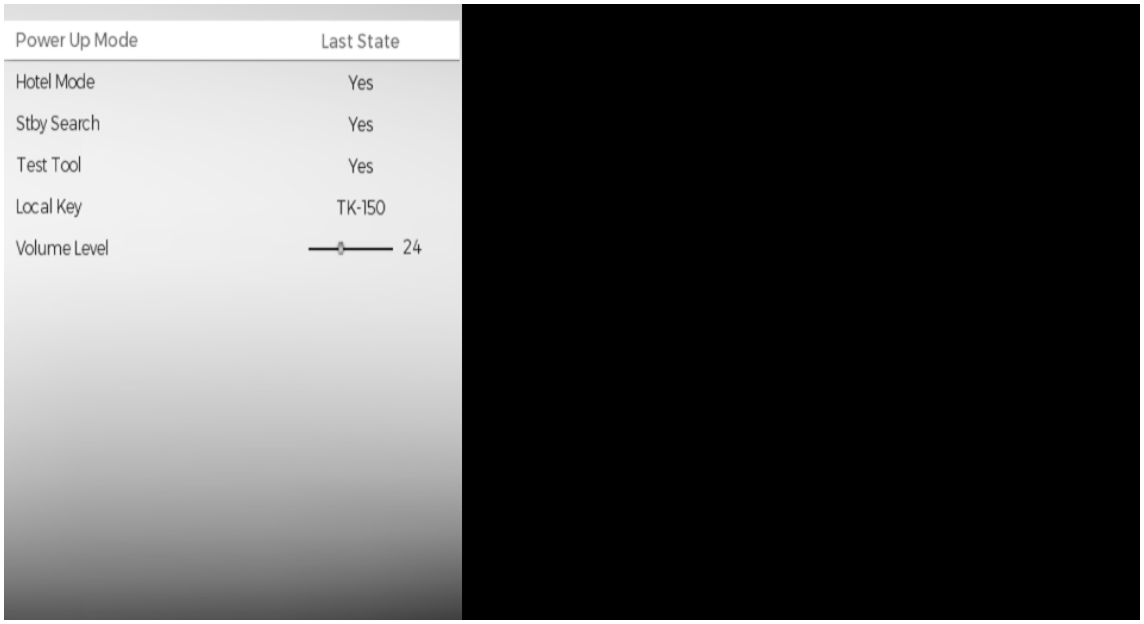
In order to reach service menu, first Press **"MENU"** buton, then write "**4725"** by using remote controller. You can see the service menu main screen below. You can check SW releases by using this menu. In addition, you can make changes on video, audio etc. by using video settings, audio settings titles.

Service Menu

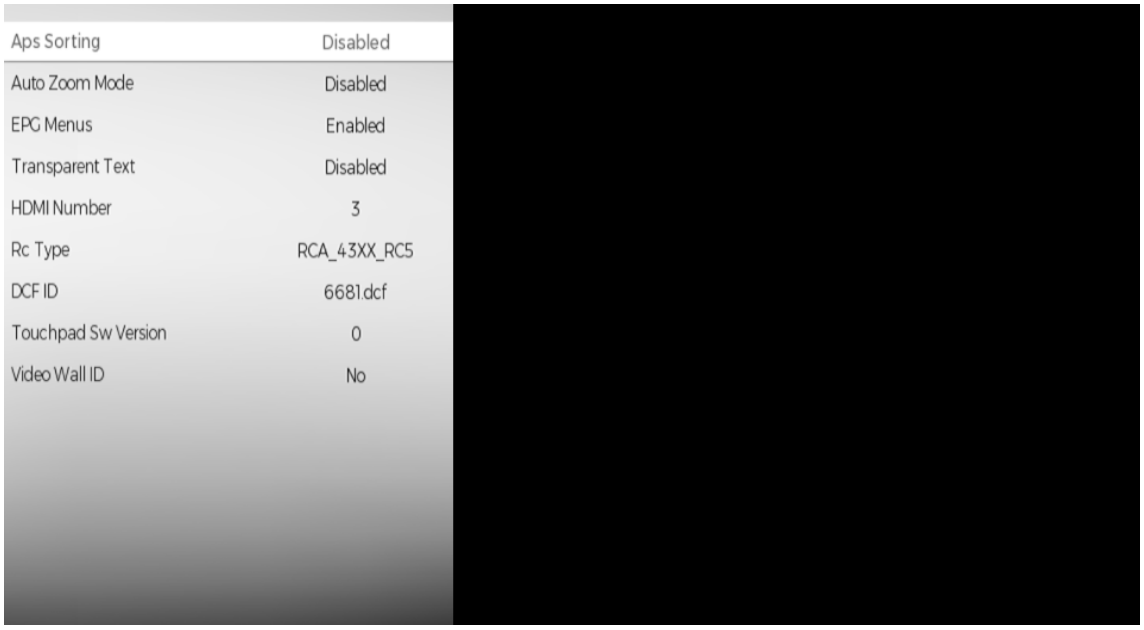
Video Settings



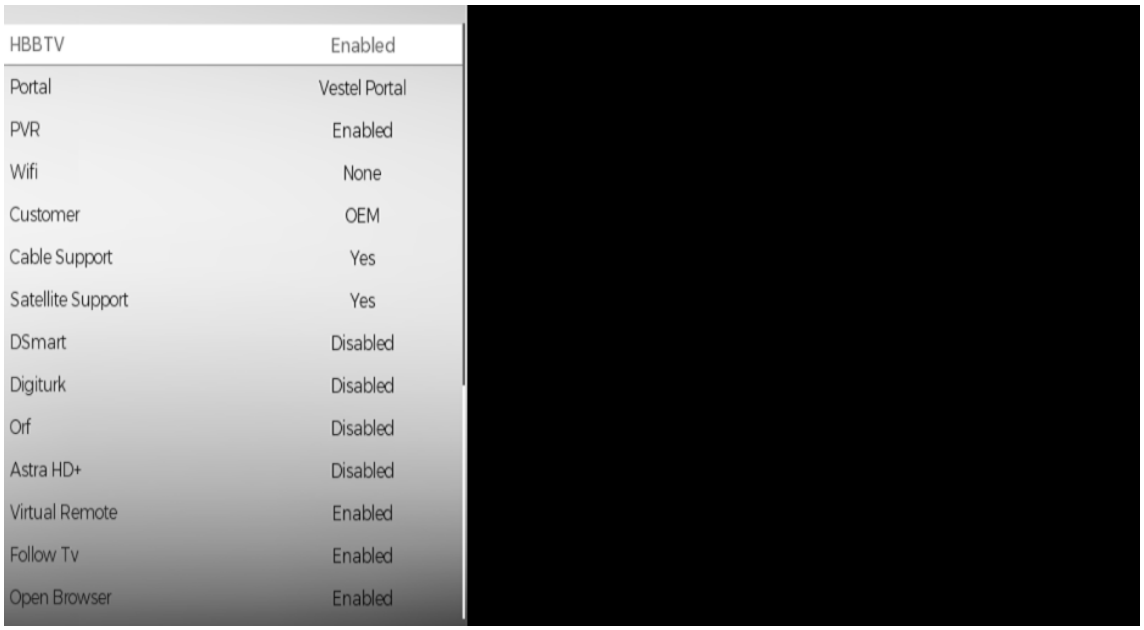
Audio Settings



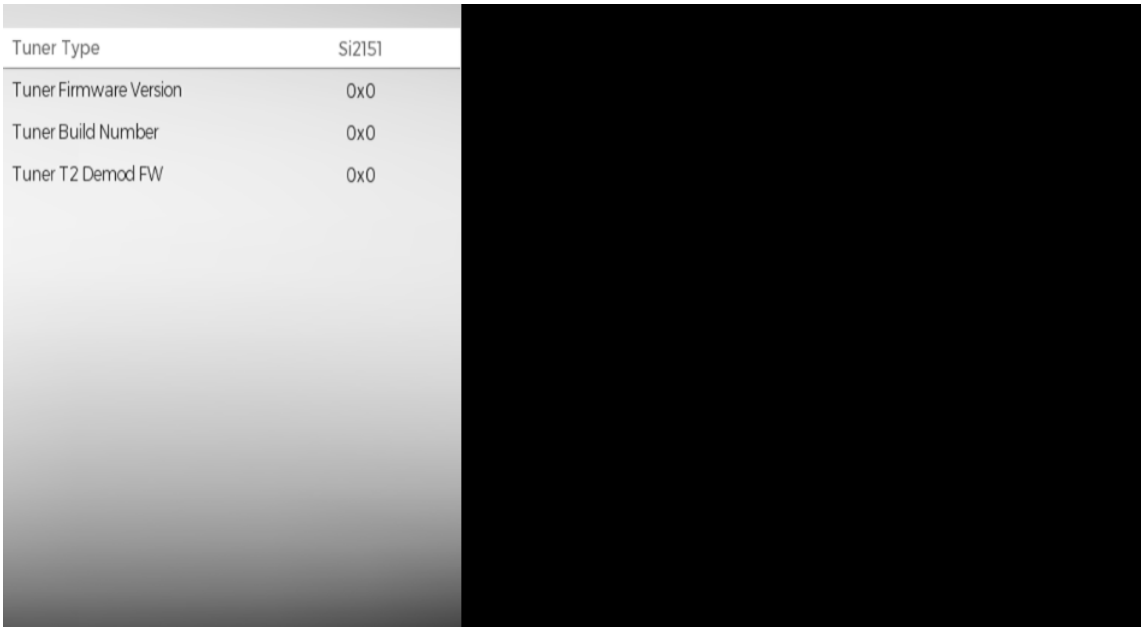
Options 1



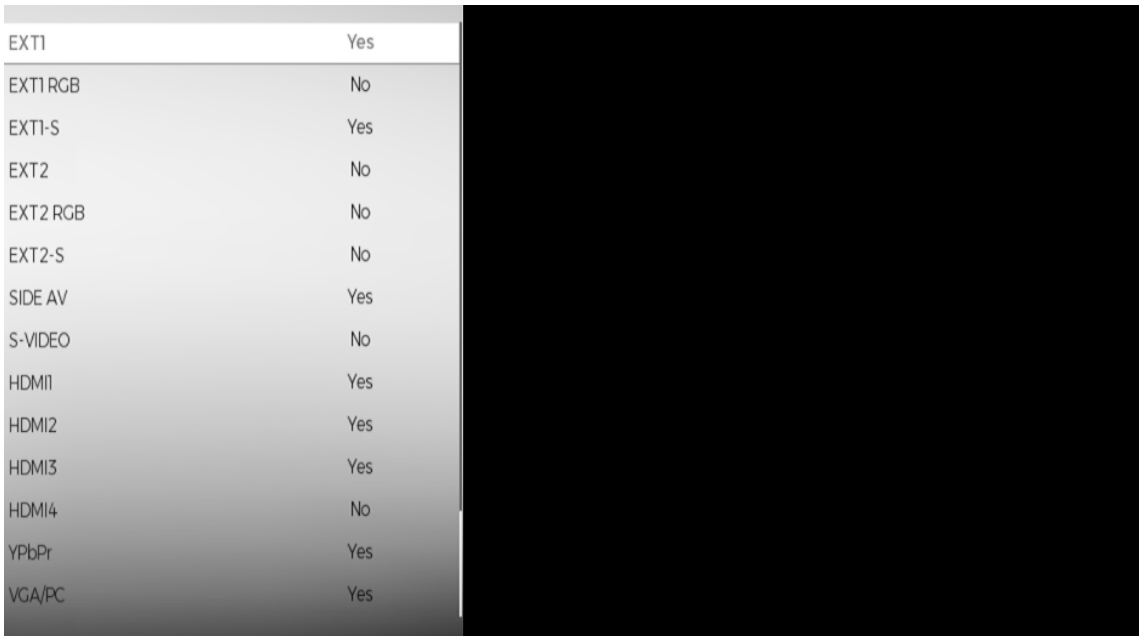
Options 2



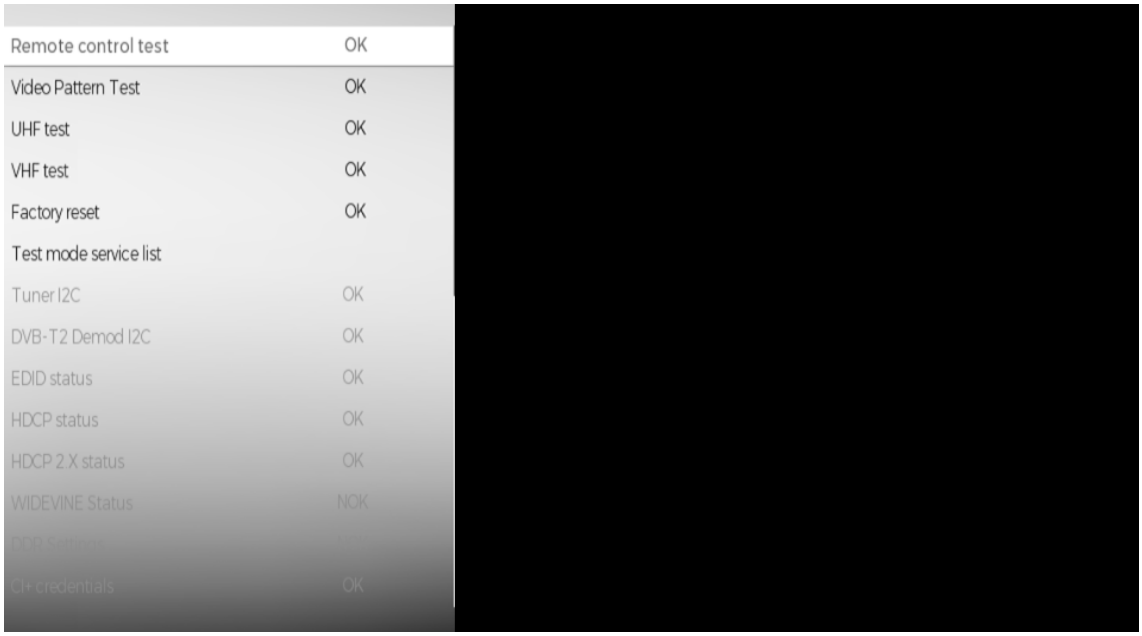
Options 3



Tuning Settings

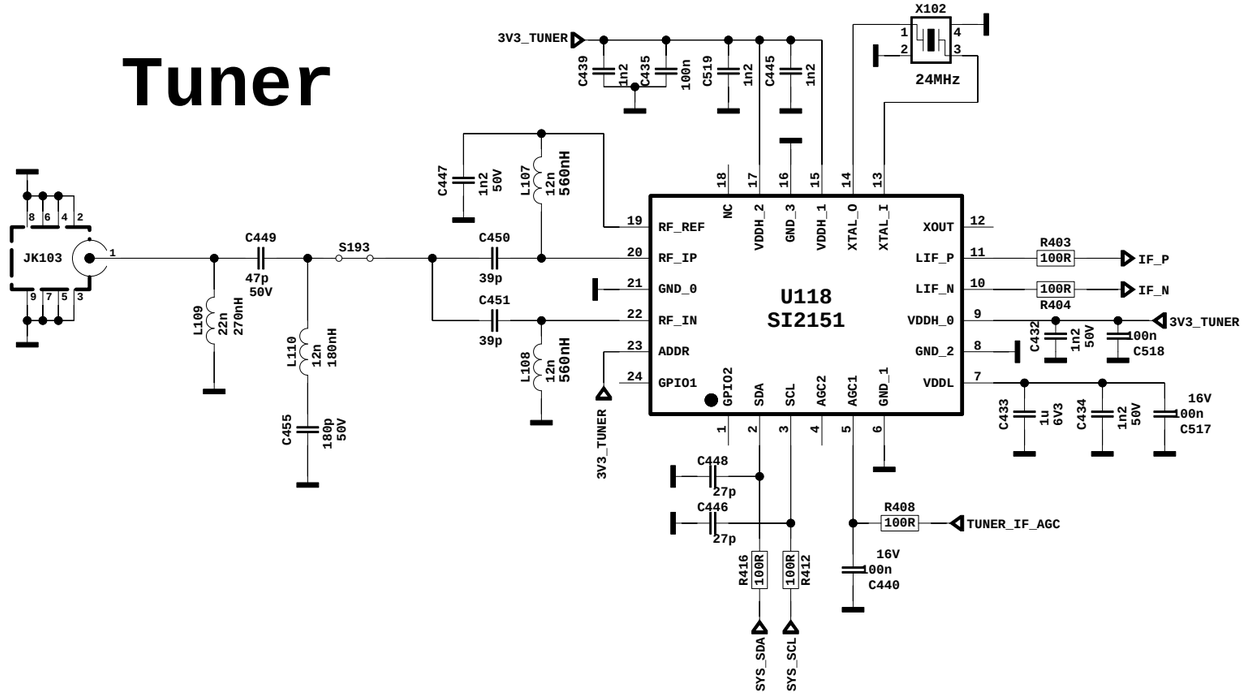


Source Settings

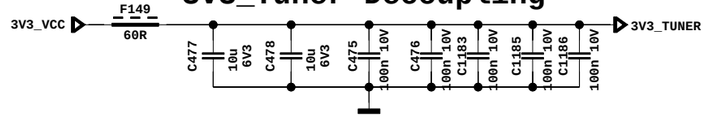

Remote control test OK
Video Pattern Test OK
UHF test OK
VHF test OK
Factory reset OK
Test mode service list
Tuner I2C OK
DVB-T2 Demod I2C OK
EDID status OK
HDCP status OK
HDCP 2.X status OK
WIDEVINE Status NOK
CI+ credentials OK

Diagnostic

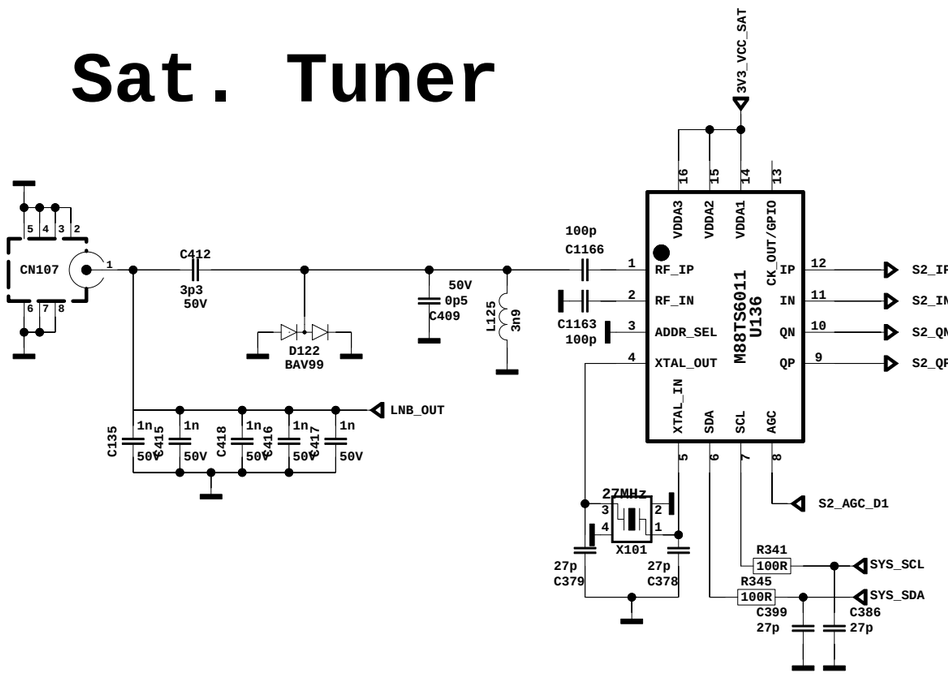
Tuner

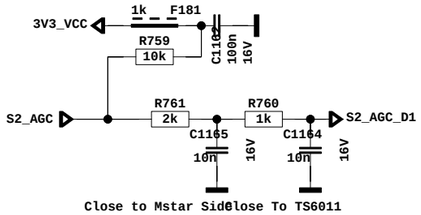


3v3_Tuner Decoupling

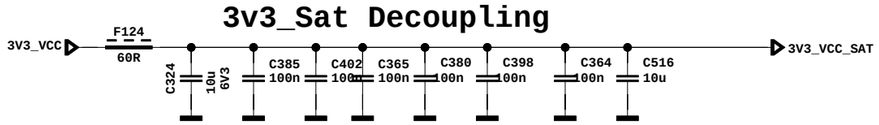


Sat. Tuner

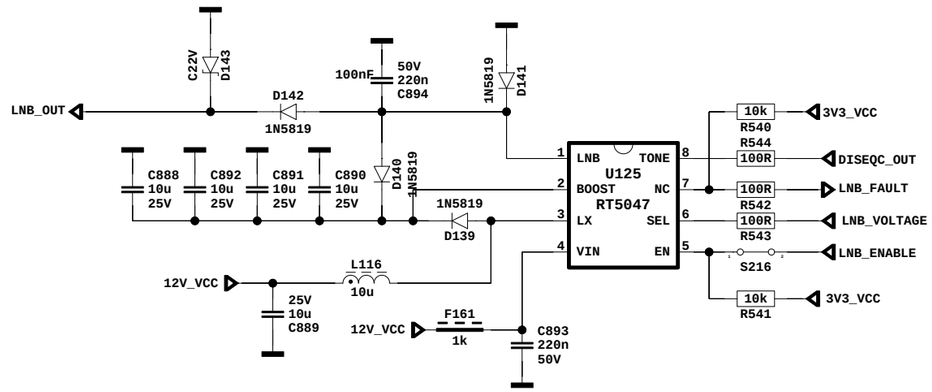




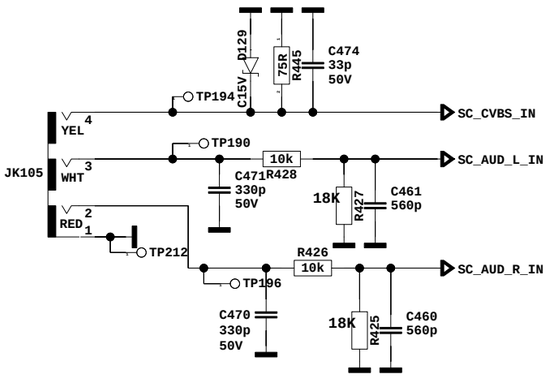
3v3_Sat Decoupling



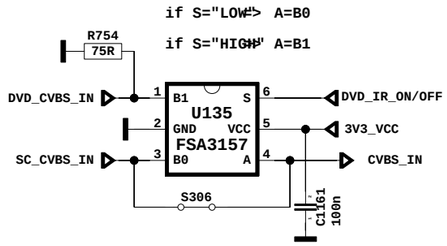
LNBp



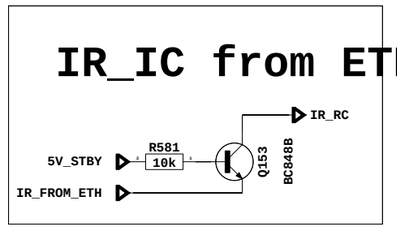
BAC AV IN



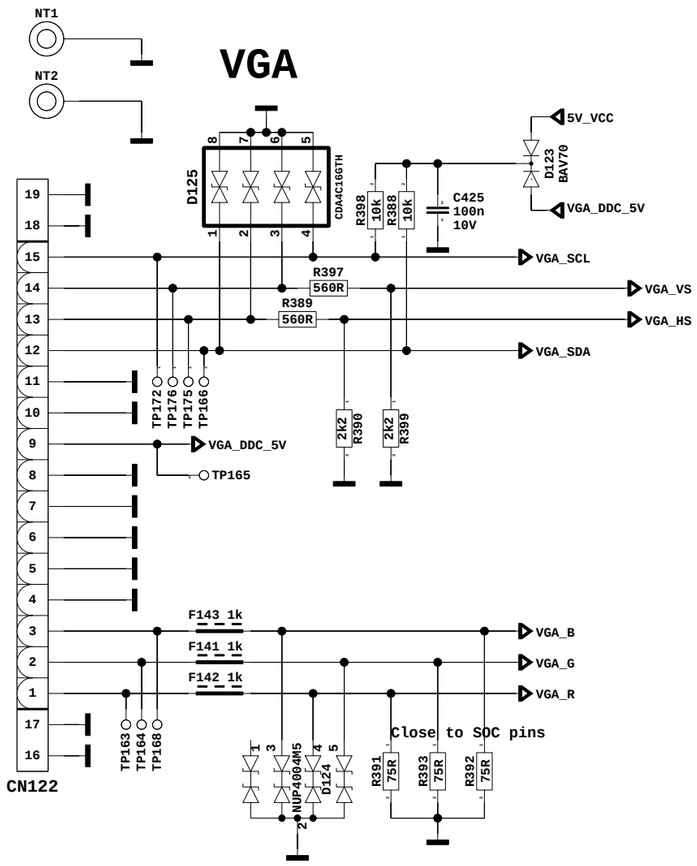
CVBS_IN Select

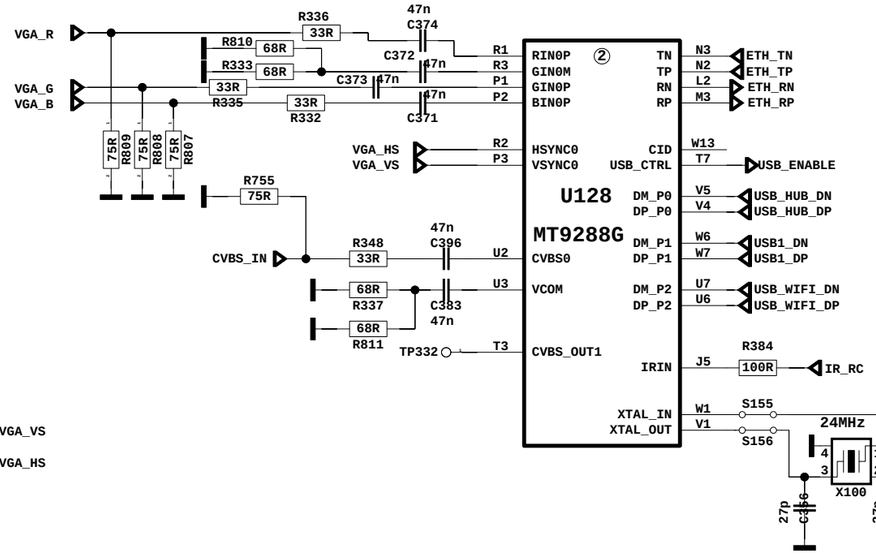


IR_IC from ETH

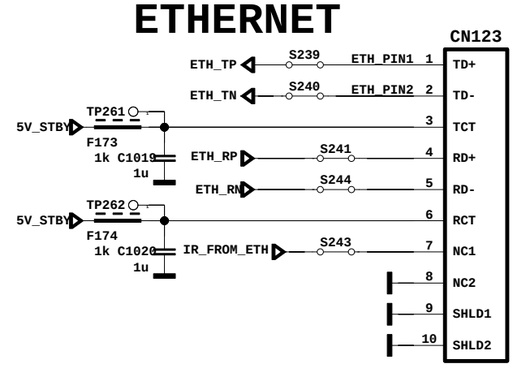


VGA

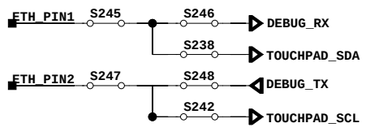




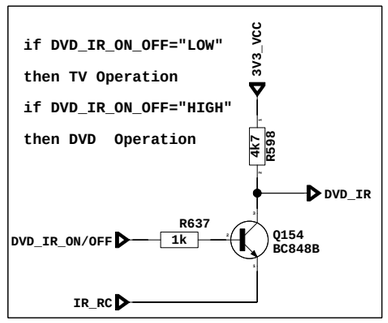
ETHERNET



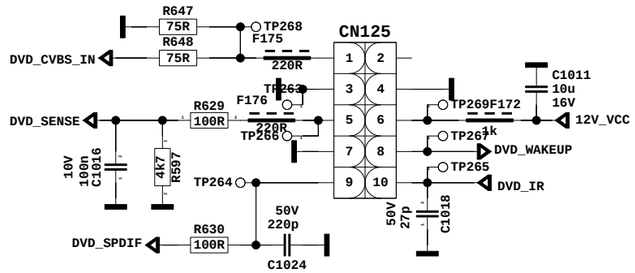
HOTEL TV OPTIONS

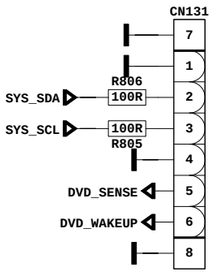


DVD IR



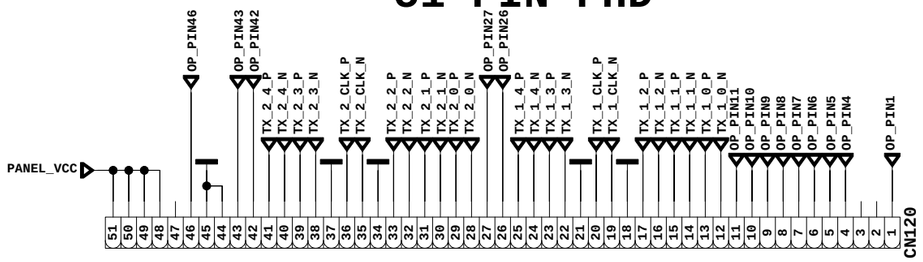
DVD INTERFACE



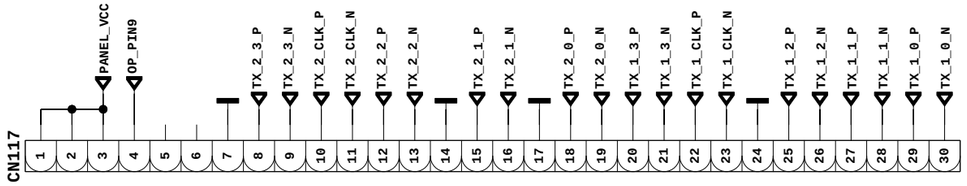


VESTEL	PROJECT NAME : 17mb181tc-r4	A3
SCH NAME :PERIPHERALs_ETH		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		26/03/2020:13:38

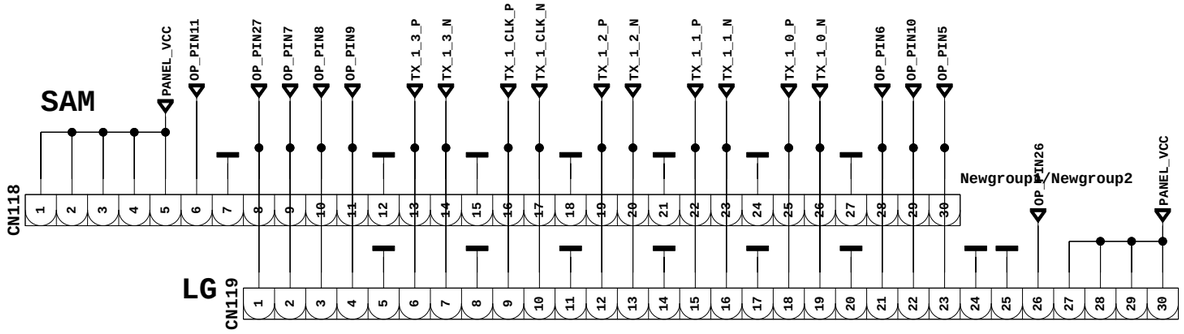
51 PIN FHD



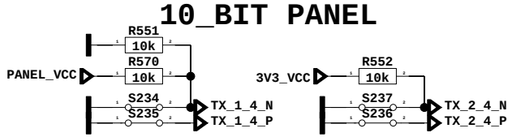
19" TO 22" DOUBLE LVDS FFC OPTIONS



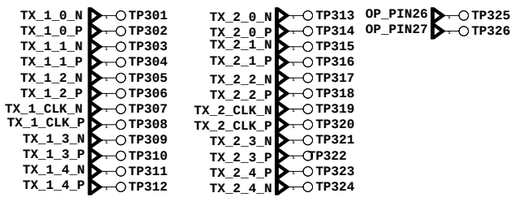
WXGA FFC



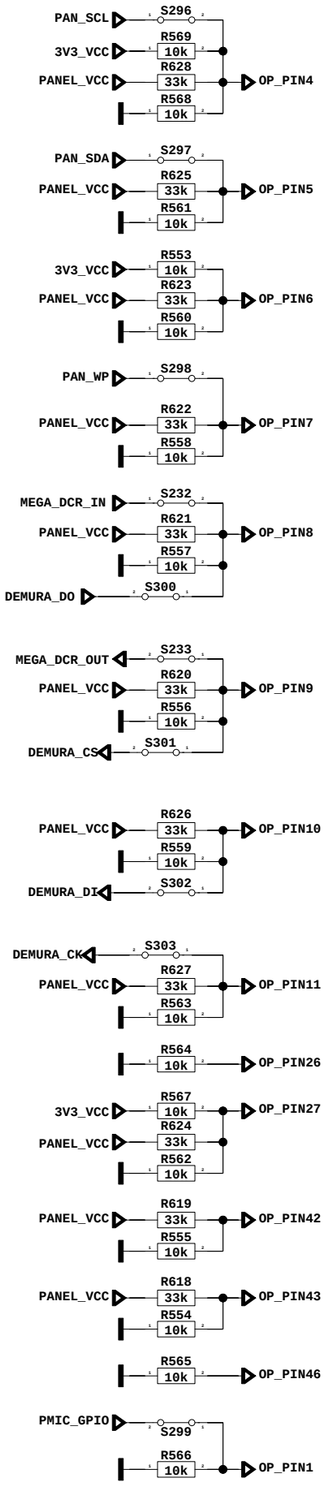
10_BIT PANEL



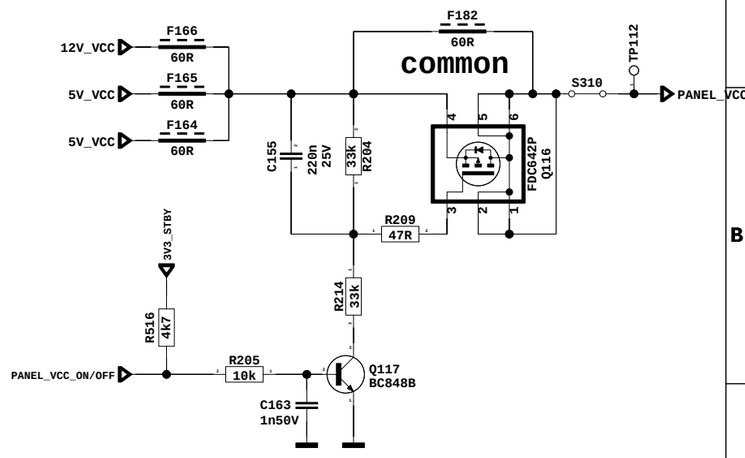
51 Pin FHD Connector Test Pins



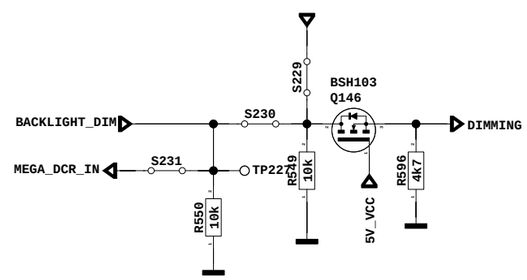
OPTIONS TABLE



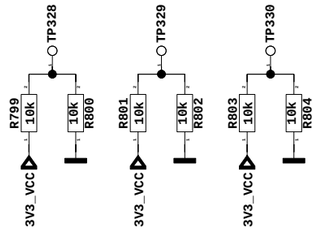
PANEL SUPPLY SWITCH



DIMMING



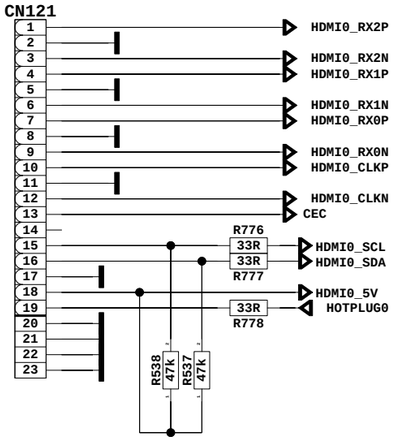
TCON SELECTION TPs



VESTEL	PROJECT NAME : 17mb181tc-r4	A3
SCH NAME :LVDS		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		18/03/2020:09:23

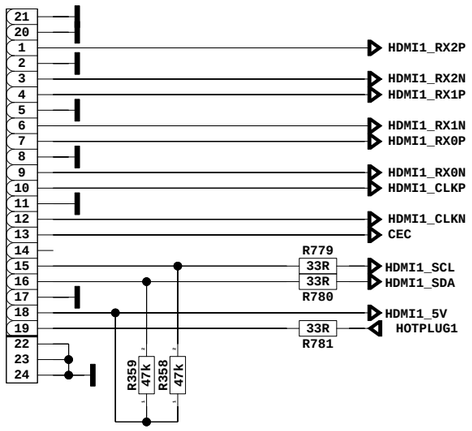
HDMI1 (SIDE)

CN121



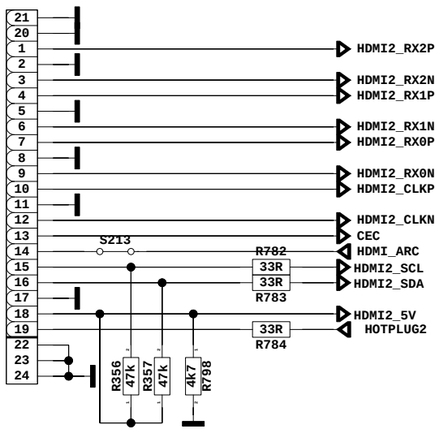
HDMI3

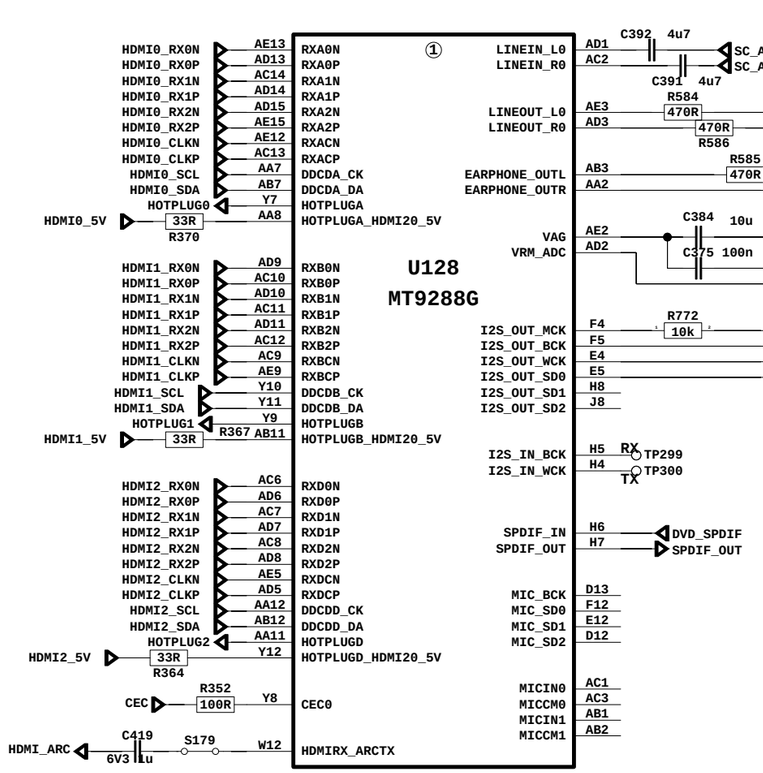
CN110



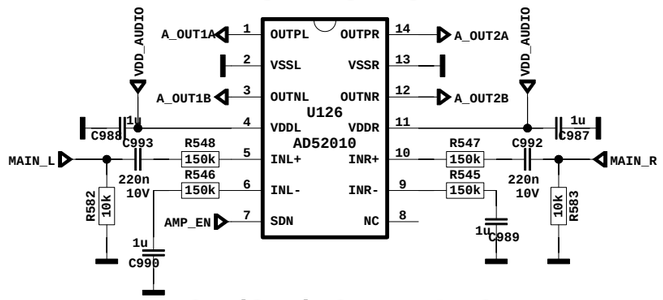
HDMI2 (W/ARC)

CN109

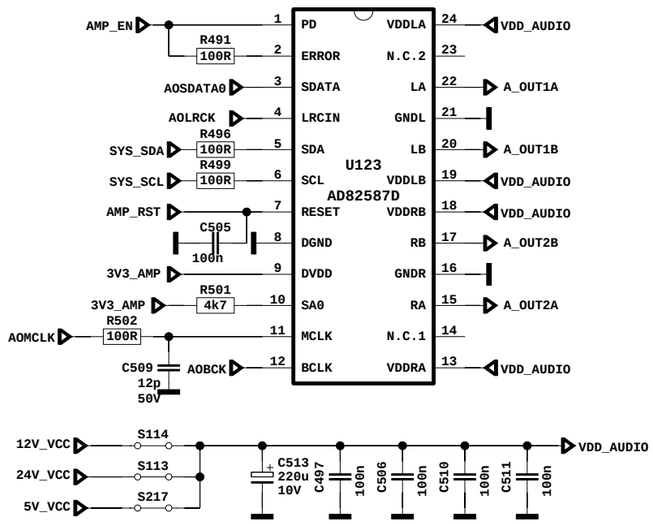




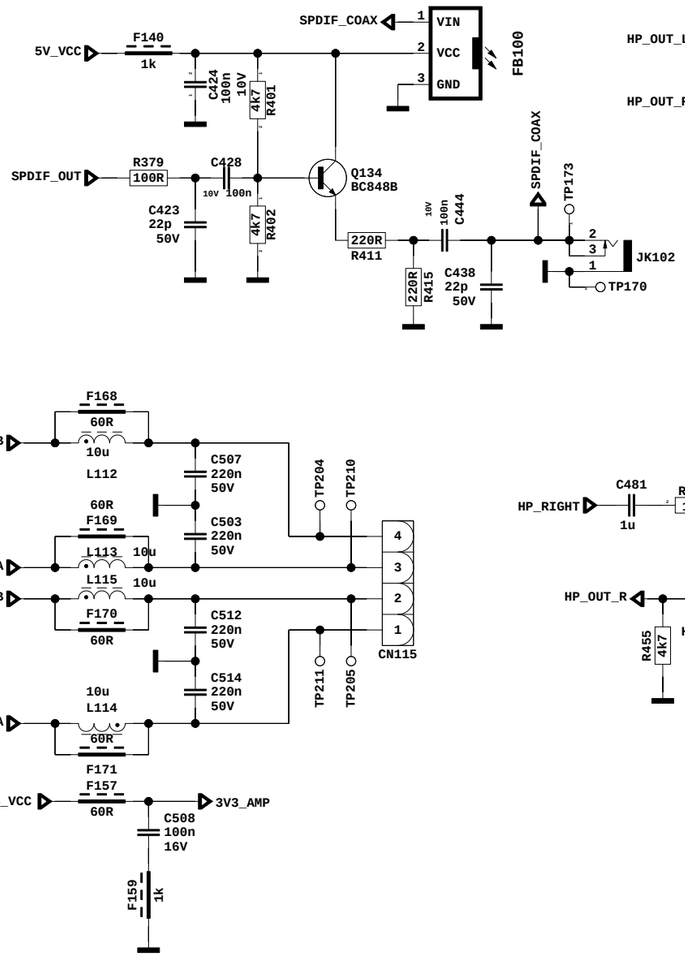
2.5W AUDIO AMP



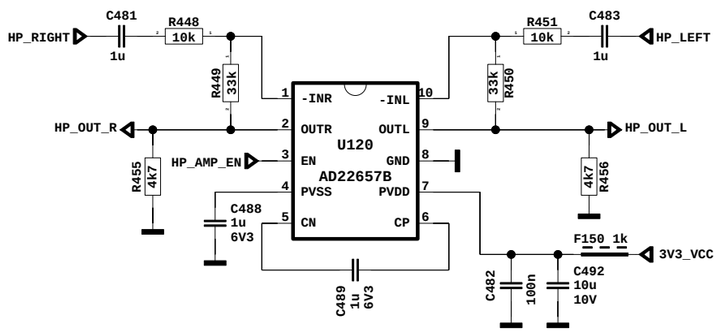
6W/8W/10W AUDIO AMP



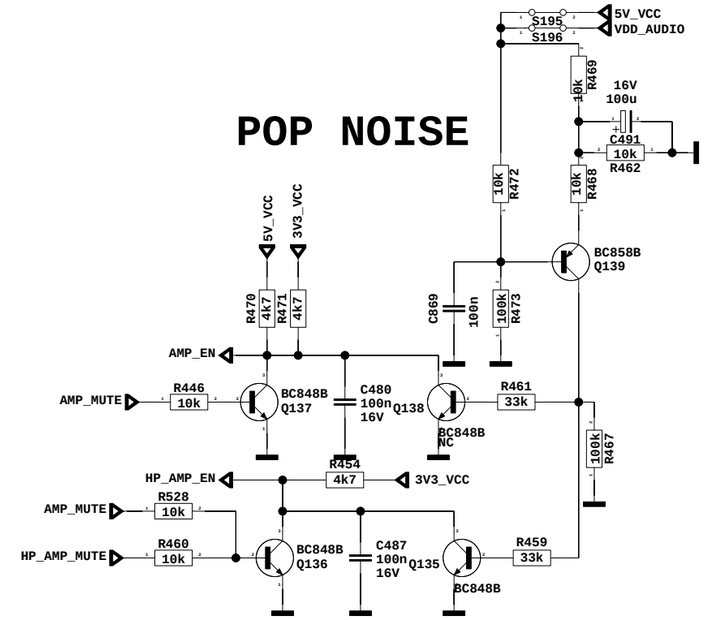
SPDIF OUT



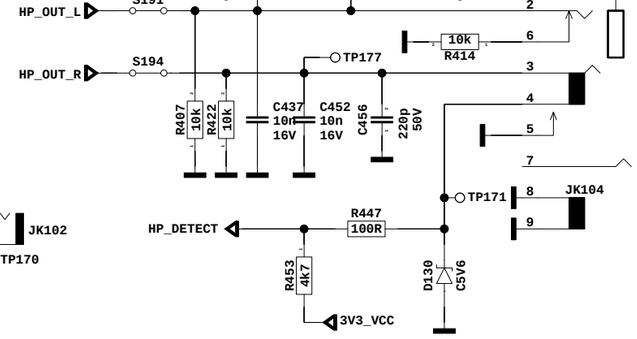
HEADPHONE AMP



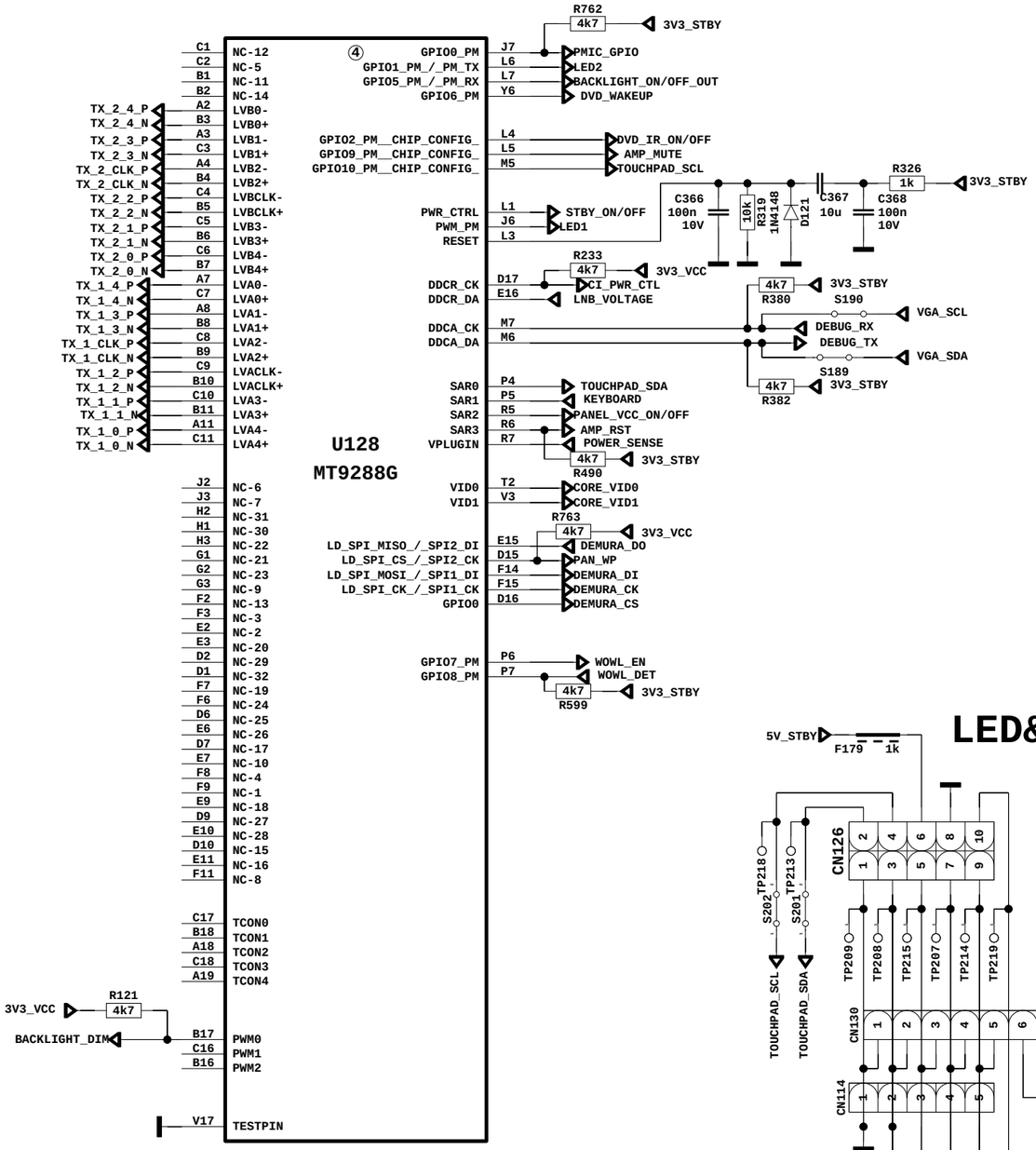
POP NOISE

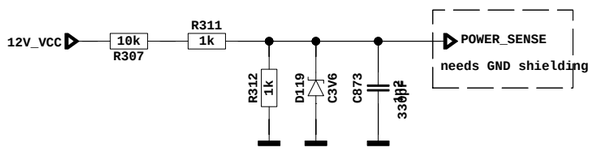


HEADPHONE OUTPUT

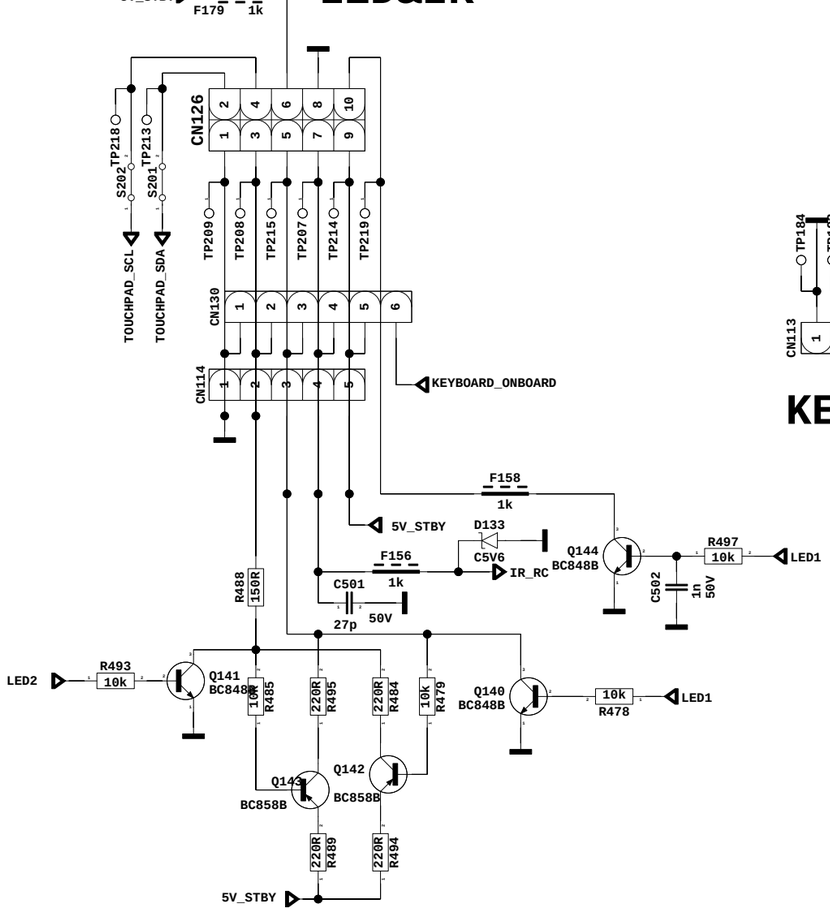


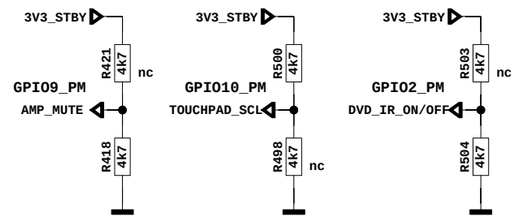
VESTEL	PROJECT NAME : 17mb181tc-r4	A3
	SCH NAME :HDMIs_AUDIO_AMPs	T. SHT 11
	DRAWN BY :<YOUR NAME HERE>	18/03/2020:09:34

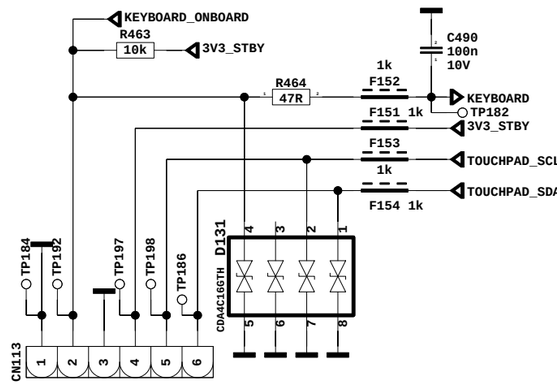




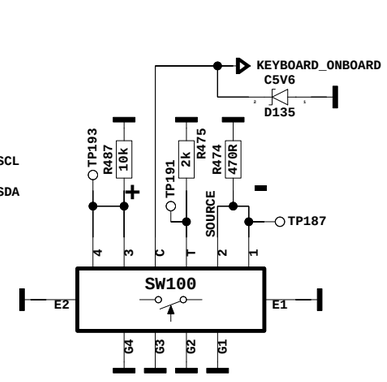
LED&IR





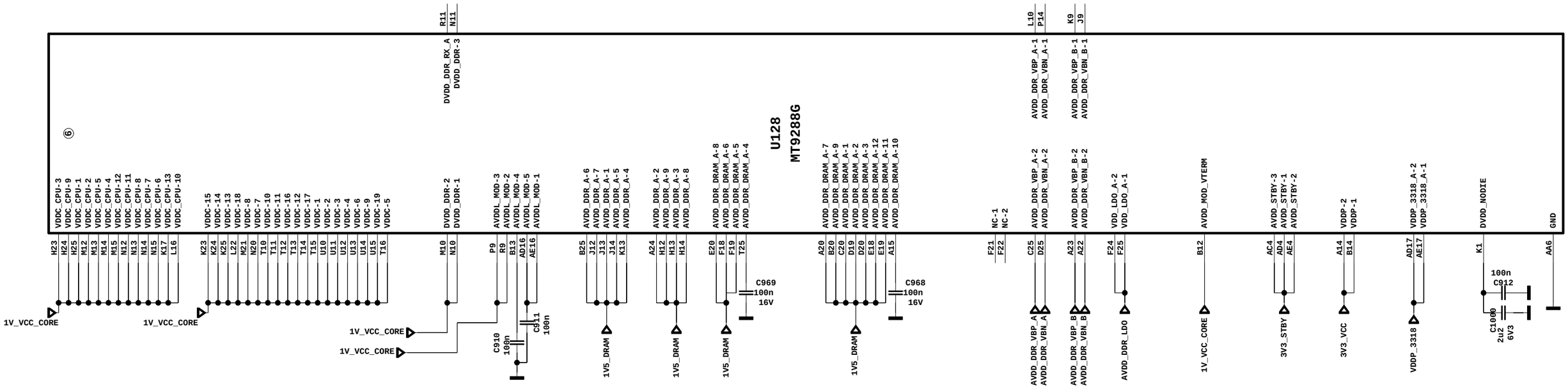


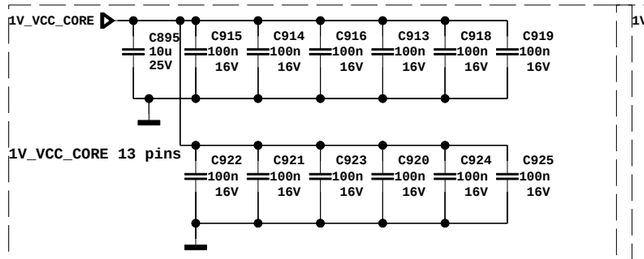
KEYBOARD

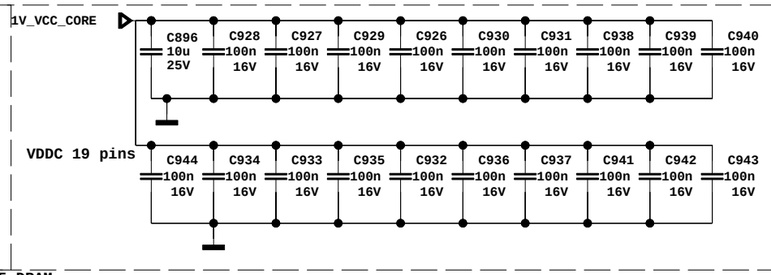


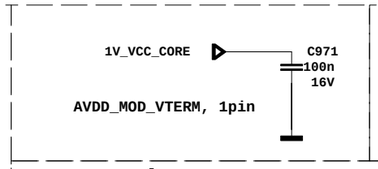
3-WAY

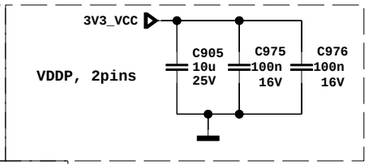
VESTEL	PROJECT NAME : 17mb181tc-r4	A3
SCH NAME :GPIOs_SPI		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		13/03/2020:09:37

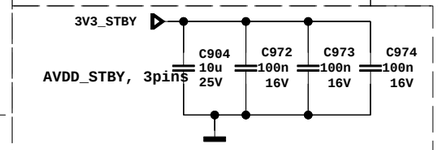

U128
MT9288G
VDDC_CPU-3
VDDC_CPU-9
VDDC_CPU-1
VDDC_CPU-2
VDDC_CPU-5
VDDC_CPU-4
VDDC_CPU-12
VDDC_CPU-11
VDDC_CPU-8
VDDC_CPU-7
VDDC_CPU-6
VDDC_CPU-13
VDDC_CPU-10
VDDC-15
VDDC-14
VDDC-13
VDDC-18
VDDC-8
VDDC-7
VDDC-10
VDDC-11
VDDC-16
VDDC-12
VDDC-17
VDDC-1
VDDC-2
VDDC-3
VDDC-4
VDDC-6
VDDC-9
VDDC-19
VDDC-5
DVDD_DDR_RX_A
DVDD_DDR-3
DVDD_DDR-2
DVDD_DDR-1
AVDDL_MOD-3
AVDDL_MOD-2
AVDDL_MOD-4
AVDDL_MOD-5
AVDDL_MOD-1
AVDD_DDR_A-6
AVDD_DDR_A-7
AVDD_DDR_A-1
AVDD_DDR_A-5
AVDD_DDR_A-4
AVDD_DDR_A-2
AVDD_DDR_A-9
AVDD_DDR_A-3
AVDD_DDR_A-8
AVDD_DDR_DRAM_A-8
AVDD_DDR_DRAM_A-6
AVDD_DDR_DRAM_A-5
AVDD_DDR_DRAM_A-4
AVDD_DDR_DRAM_A-7
AVDD_DDR_DRAM_A-9
AVDD_DDR_DRAM_A-1
AVDD_DDR_DRAM_A-2
AVDD_DDR_DRAM_A-3
AVDD_DDR_DRAM_A-12
AVDD_DDR_DRAM_A-11
AVDD_DDR_DRAM_A-10
NC-1
NC-2
AVDD_DDR_VBP_A-1
AVDD_DDR_VBM_A-1
AVDD_DDR_VBP_B-1
AVDD_DDR_VBM_B-1
AVDD_DDR_VBP_A-2
AVDD_DDR_VBN_A-2
AVDD_DDR_VBP_B-2
AVDD_DDR_VBN_B-2
VDD_LDO_A-2
VDD_LDO_A-1
AVDD_MOD_VTERM
AVDD_STBY-3
AVDD_STBY-1
AVDD_STBY-2
VDDP-2
VDDP-1
VDDP_3318_A-2
VDDP_3318_A-1
DVDD_NODIE
GND
1V_VCC_CORE
1V5_DRAM
AVDD_DDR_VBP_A
AVDD_DDR_VBN_A
AVDD_DDR_VBP_B
AVDD_DDR_VBN_B
AVDD_DDR_LDO
3V3_STBY
3V3_VCC
VDDP_3318
C969 100n 16V
C968 100n 16V
C911 100n
C910 100n
C912 100n
C1000 2u2 6V3

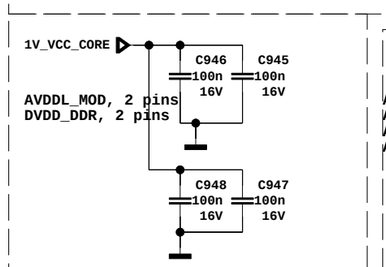

1V_VCC_CORE
C895 10u 25V
C915 100n 16V
C914 100n 16V
C916 100n 16V
C913 100n 16V
C918 100n 16V
C919 100n 16V
1V_VCC_CORE 13 pins
C922 100n 16V
C921 100n 16V
C923 100n 16V
C920 100n 16V
C924 100n 16V
C925 100n 16V

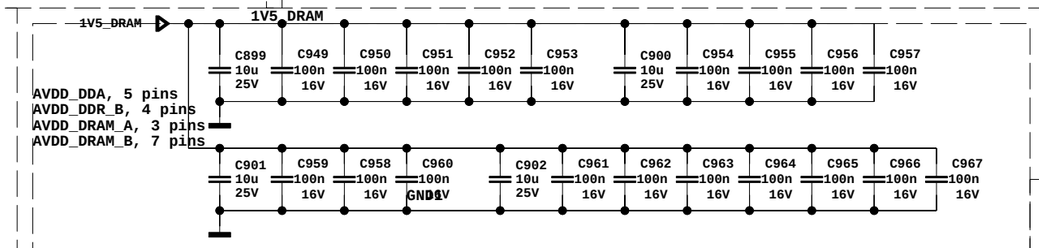

1V_VCC_CORE
C896 10u 25V
C928 100n 16V
C927 100n 16V
C929 100n 16V
C926 100n 16V
C930 100n 16V
C931 100n 16V
C938 100n 16V
C939 100n 16V
C940 100n 16V
VDDC 19 pins
C944 100n 16V
C934 100n 16V
C933 100n 16V
C935 100n 16V
C932 100n 16V
C936 100n 16V
C937 100n 16V
C941 100n 16V
C942 100n 16V
C943 100n 16V

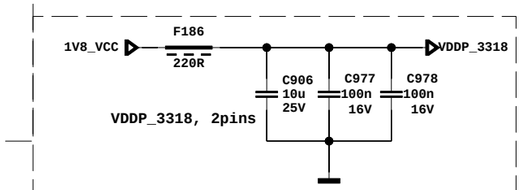

1V_VCC_CORE
C971 100n 16V
AVDD_MOD_VTERM, 1pin

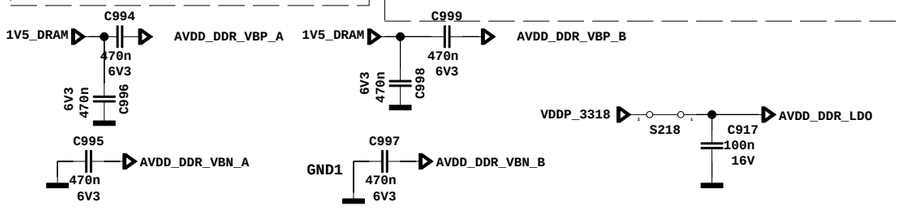

3V3_VCC
C905 10u 25V
C975 100n 16V
C976 100n 16V
VDDP, 2pins

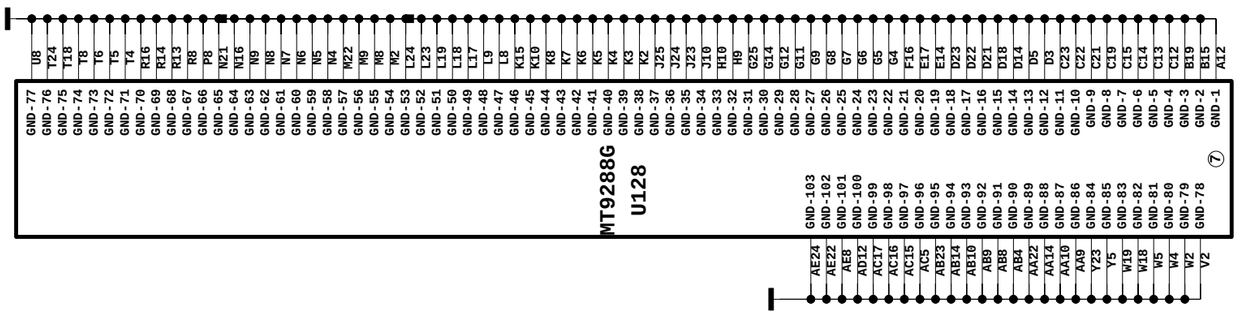

3V3_STBY
C904 10u 25V
C972 100n 16V
C973 100n 16V
C974 100n 16V
AVDD_STBY, 3pins


1V_VCC_CORE
C946 100n 16V
C945 100n 16V
AVDDL_MOD, 2 pins
DVDD_DDR, 2 pins
C948 100n 16V
C947 100n 16V


1V5_DRAM
1V5_DRAM
C899 10u 25V
C949 100n 16V
C950 100n 16V
C951 100n 16V
C952 100n 16V
C953 100n 16V
C900 10u 25V
C954 100n 16V
C955 100n 16V
C956 100n 16V
C957 100n 16V
AVDD_DDA, 5 pins
AVDD_DDR_B, 4 pins
AVDD_DRAM_A, 3 pins
AVDD_DRAM_B, 7 pins
C901 10u 25V
C959 100n 16V
C958 100n 16V
C960 100n 16V
GND1
C902 10u 25V
C961 100n 16V
C962 100n 16V
C963 100n 16V
C964 100n 16V
C965 100n 16V
C966 100n 16V
C967 100n 16V


1V8_VCC
F186
220R
VDDP_3318
C906 10u 25V
C977 100n 16V
C978 100n 16V
VDDP_3318, 2pins


1V5_DRAM
C994 470n 6V3
AVDD_DDR_VBP_A
6V3 470n C996
C995 470n 6V3
AVDD_DDR_VBN_A
1V5_DRAM
C999 470n 6V3
AVDD_DDR_VBP_B
6V3 470n C998
GND1
C997 470n 6V3
AVDD_DDR_VBN_B
VDDP_3318
S218
C917 100n 16V
AVDD_DDR_LDO


U128
MT9288G
GND-77
GND-76
GND-75
GND-74
GND-73
GND-72
GND-71
GND-70
GND-69
GND-68
GND-67
GND-66
GND-65
GND-64
GND-63
GND-62
GND-61
GND-60
GND-59
GND-58
GND-57
GND-56
GND-55
GND-54
GND-53
GND-52
GND-51
GND-50
GND-49
GND-48
GND-47
GND-46
GND-45
GND-44
GND-43
GND-42
GND-41
GND-40
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GND-38
GND-37
GND-36
GND-35
GND-34
GND-33
GND-32
GND-31
GND-30
GND-29
GND-28
GND-27
GND-26
GND-25
GND-24
GND-23
GND-22
GND-21
GND-20
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GND-18
GND-17
GND-16
GND-15
GND-14
GND-13
GND-12
GND-11
GND-10
GND-9
GND-8
GND-7
GND-6
GND-5
GND-4
GND-3
GND-2
GND-1
GND-103
GND-102
GND-101
GND-100
GND-99
GND-98
GND-97
GND-96
GND-95
GND-94
GND-93
GND-92
GND-91
GND-90
GND-89
GND-88
GND-87
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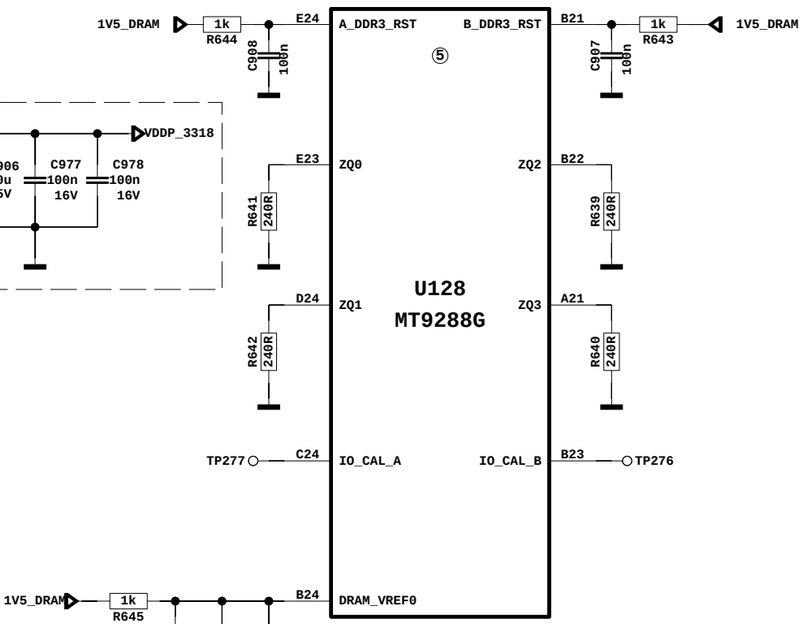
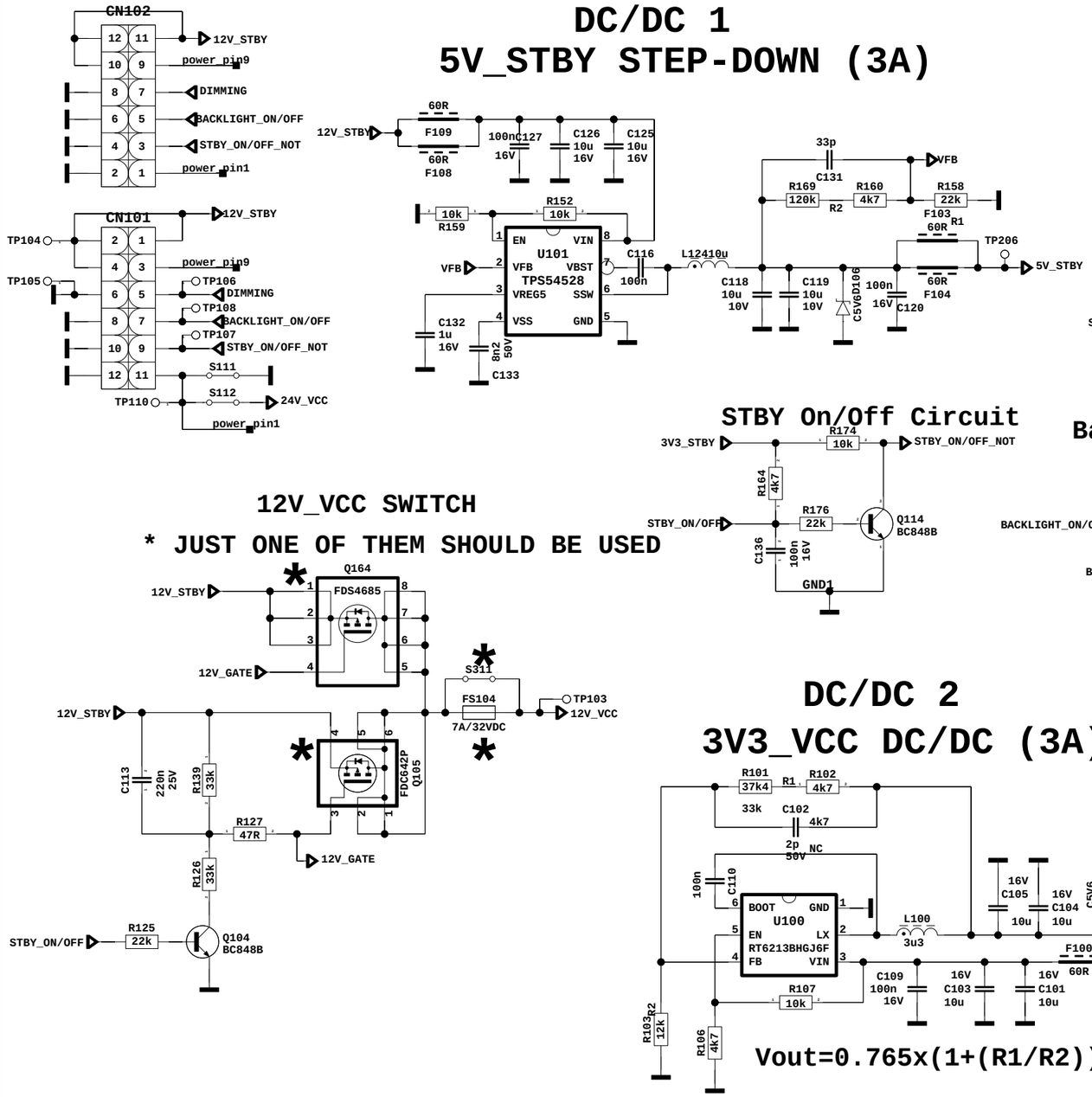
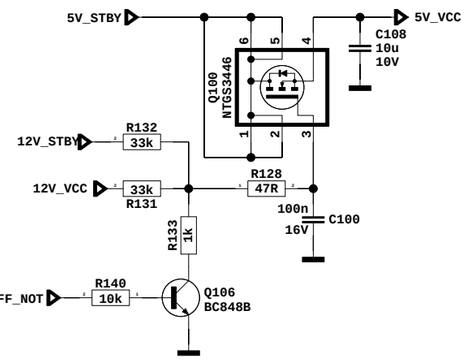
GND-82
GND-81
GND-80
GND-79
GND-78


1V5_DRAM
1k R644
C908 100n
1k R643
C907 100n
1V5_DRAM
A_DDR3_RST
B_DDR3_RST
ZQ0
ZQ2
ZQ1
ZQ3
R641 240R
R639 240R
R642 240R
R640 240R
U128
MT9288G
TP277
C24
IO_CAL_A
IO_CAL_B
B23
TP276
1V5_DRAM
1k R645
R646 1k
100n C909
C1023 1n
DRAM_VREF0

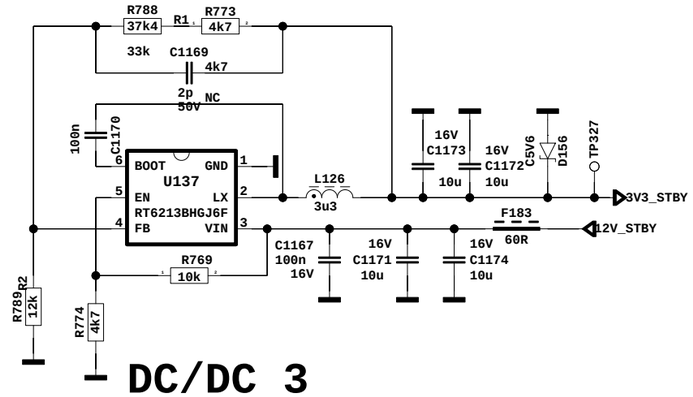
DC/DC 1
5V_STBY STEP-DOWN (3A)



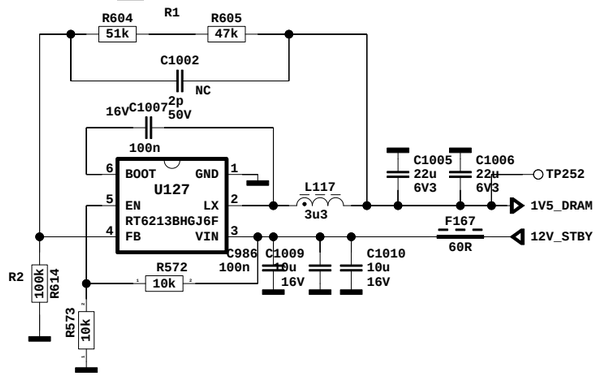
SW2
5V_VCC SWITCH



3V3_STBY DC/DC (2A)

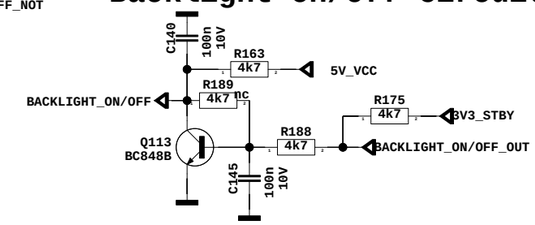


DC/DC 3
1V5_DRAM DC/DC



STBY On/Off Circuit

Backlight On/Off Circuit

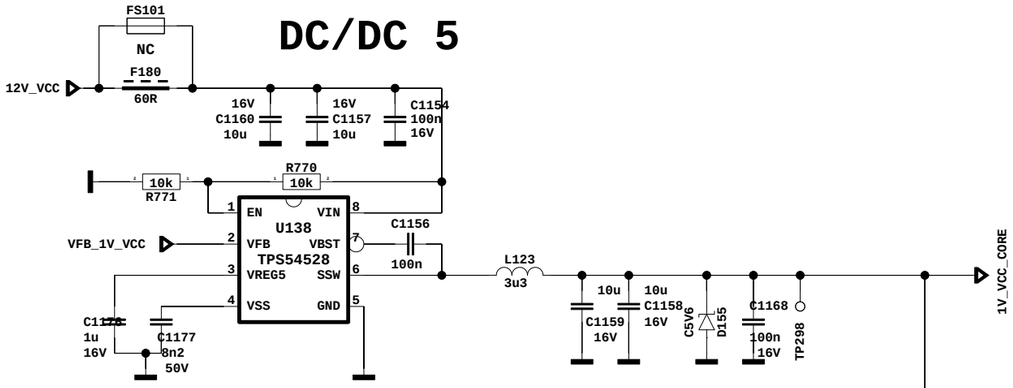


12V_VCC SWITCH
* JUST ONE OF THEM SHOULD BE USED

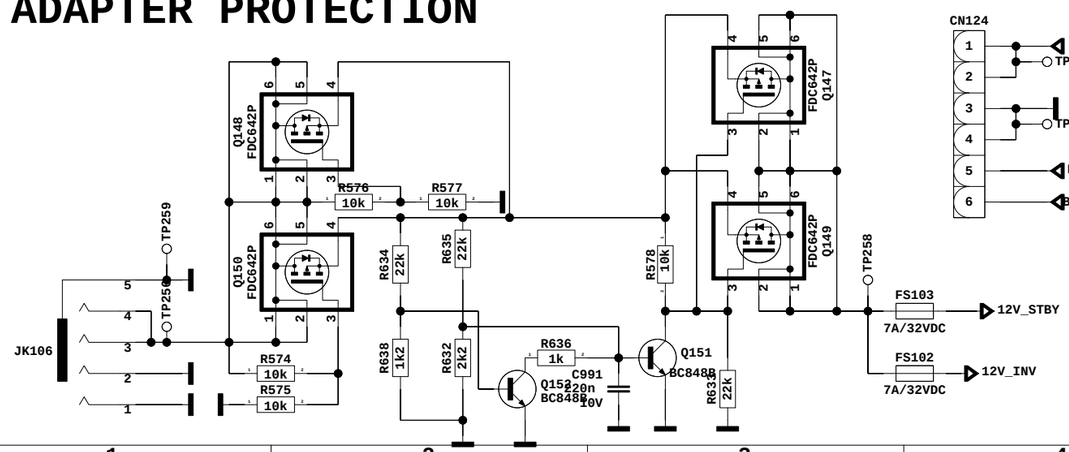
DC/DC 2
3V3_VCC DC/DC (3A)

Vout=0.765x(1+(R1/R2))

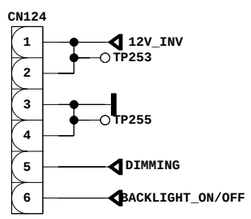
1V_VCC_CORE DC/DC (5A)
DC/DC 5



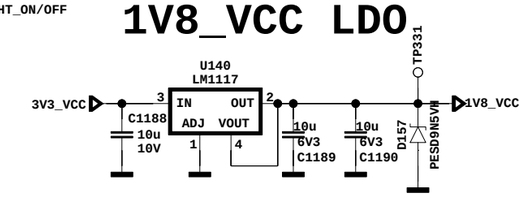
ADAPTER PROTECTION



Converter Socket

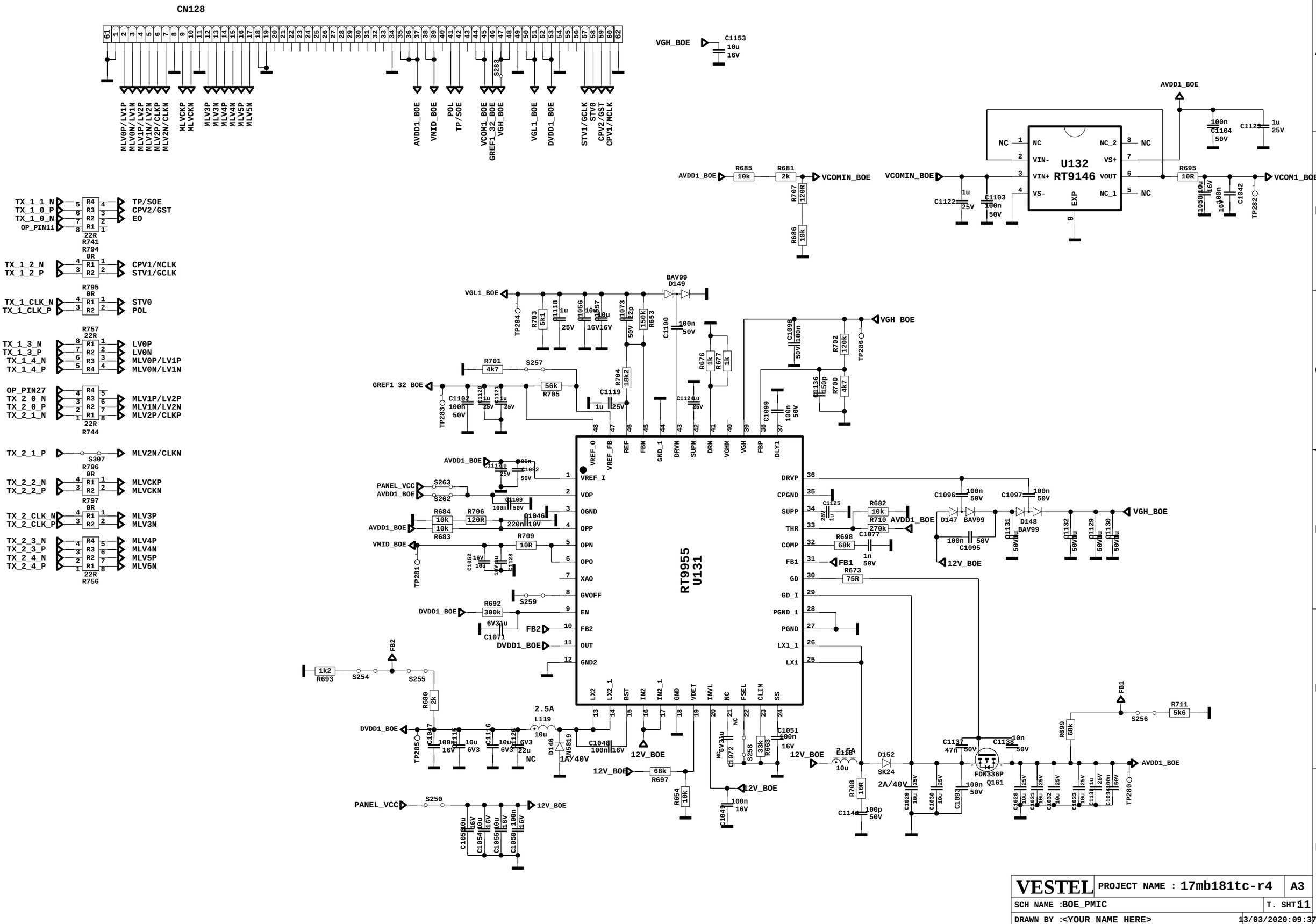


1V8_VCC LDO



Vestel

PROJECT NAME : 17mb181tc-r4		A3
SCH NAME :POWER	T. SHT	11
DRAWN BY :<YOUR NAME HERE>	18/03/2020:10:06	



VESTEL	PROJECT NAME : 17mb181tc-r4		A3
SCH NAME :BOE_PMIC		T. SHT	11
DRAWN BY :<YOUR NAME HERE>		13/03/2020:09:37	

VGL BLOCK

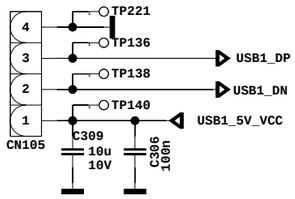
VGH BLOCK

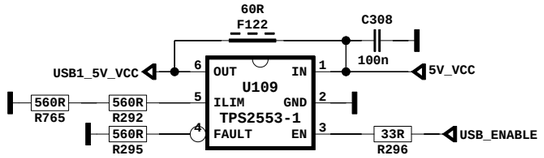
PANEL I2C BUFFER

RT6919B
U134

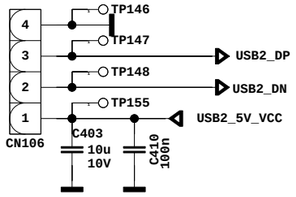
VESTEL	PROJECT NAME : 17mb181tc-r4	A3	
SCH NAME :LG_PMIC		T. SHT	11
DRAWN BY :<YOUR NAME HERE>		13/03/2020:09:37	

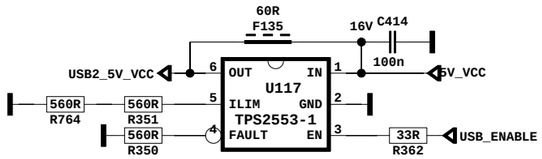
USB1 2.0



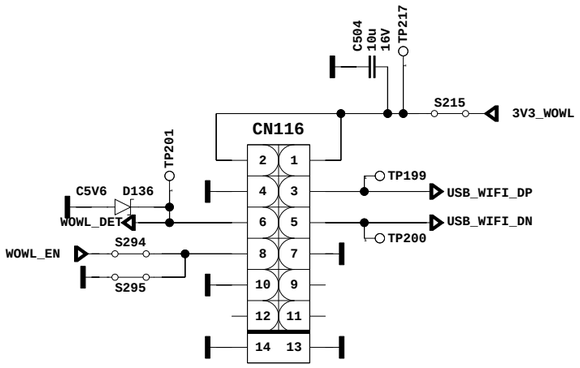


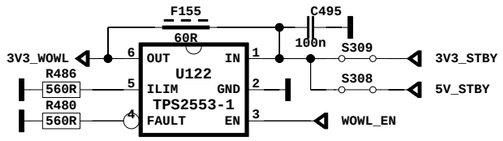
USB2 2.0



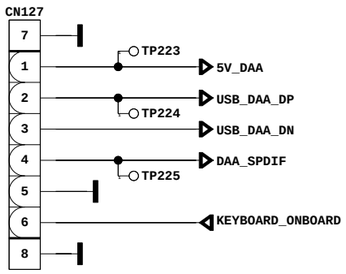


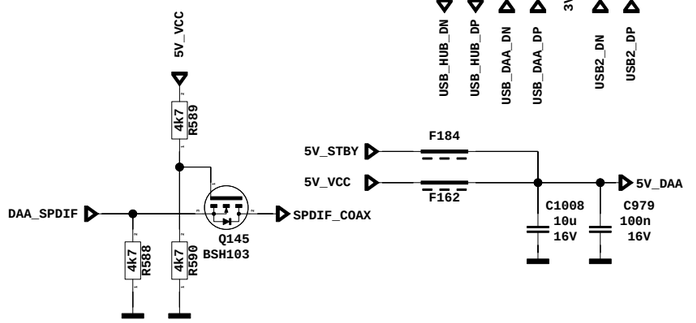
WIFI&BT



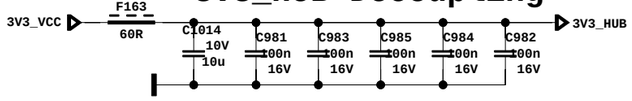


DAA INTERFACE

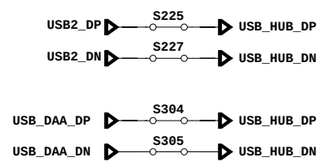




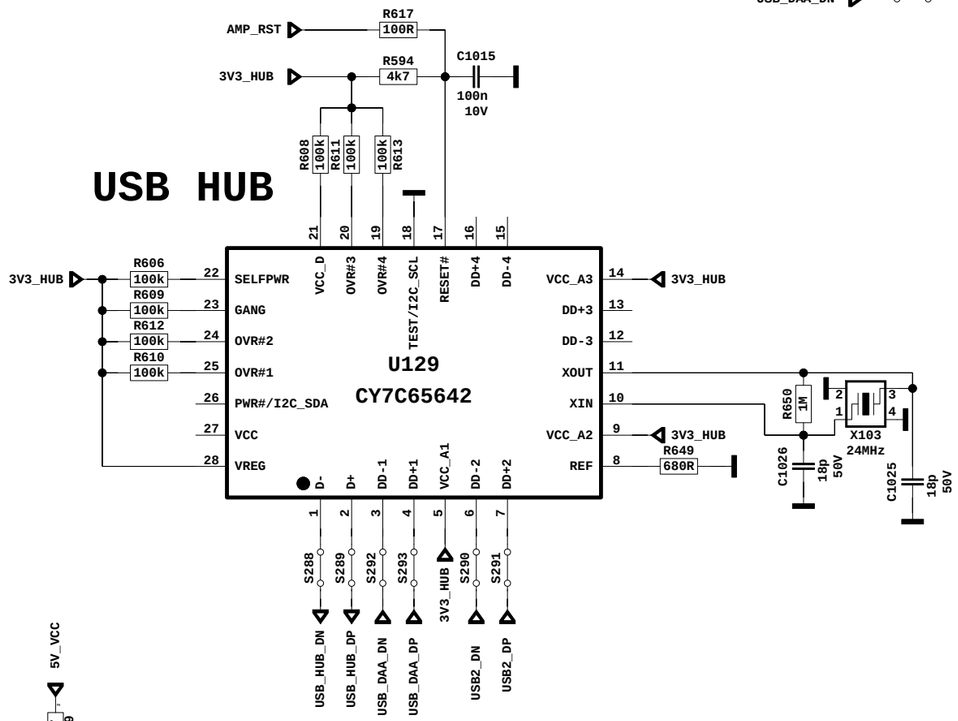
3v3_HUB Decoupling

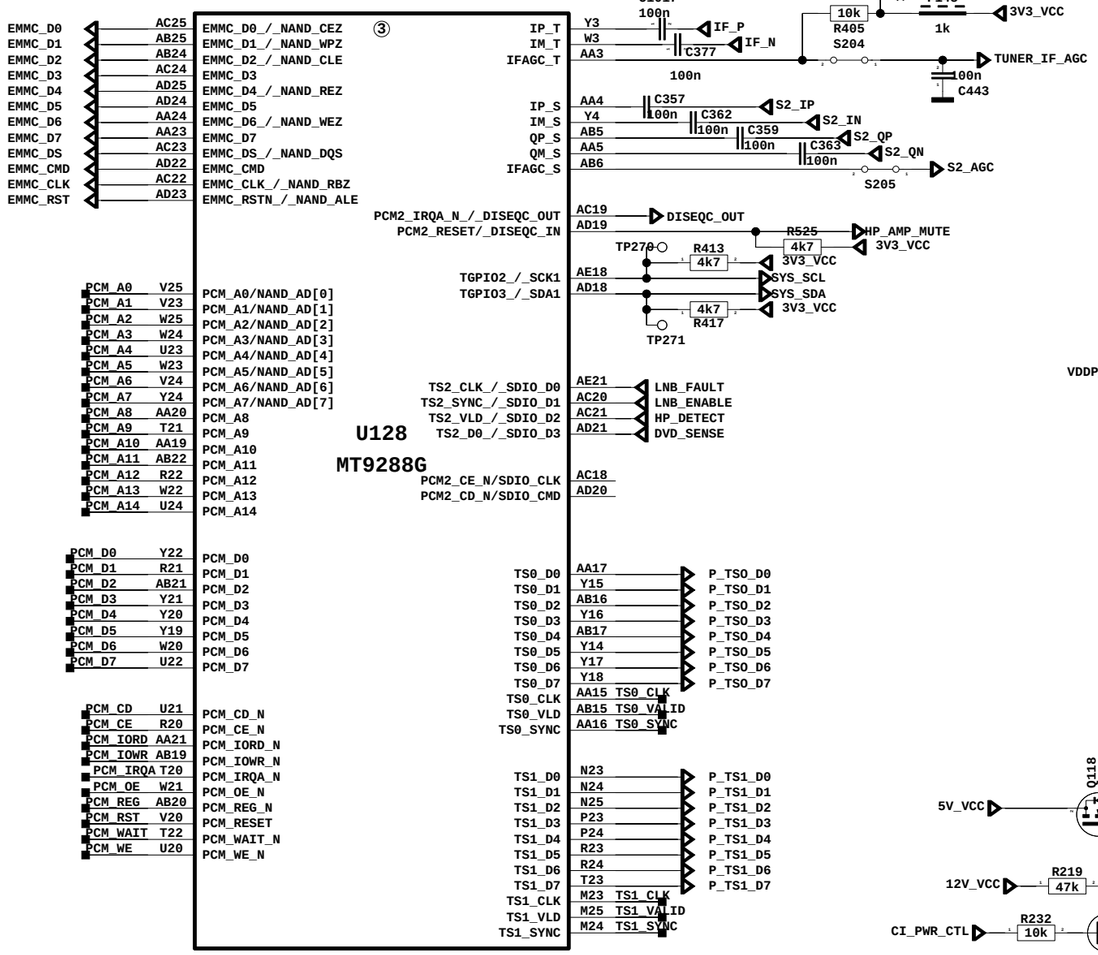


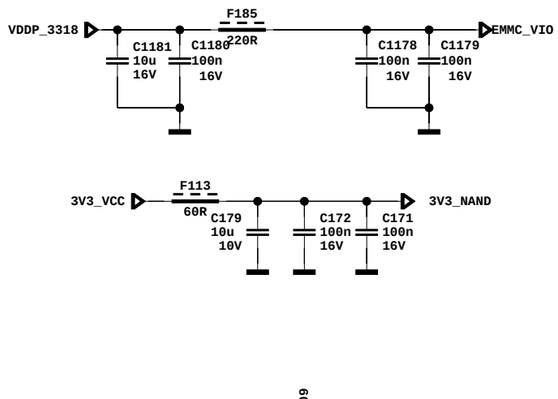
HUB BYPASS

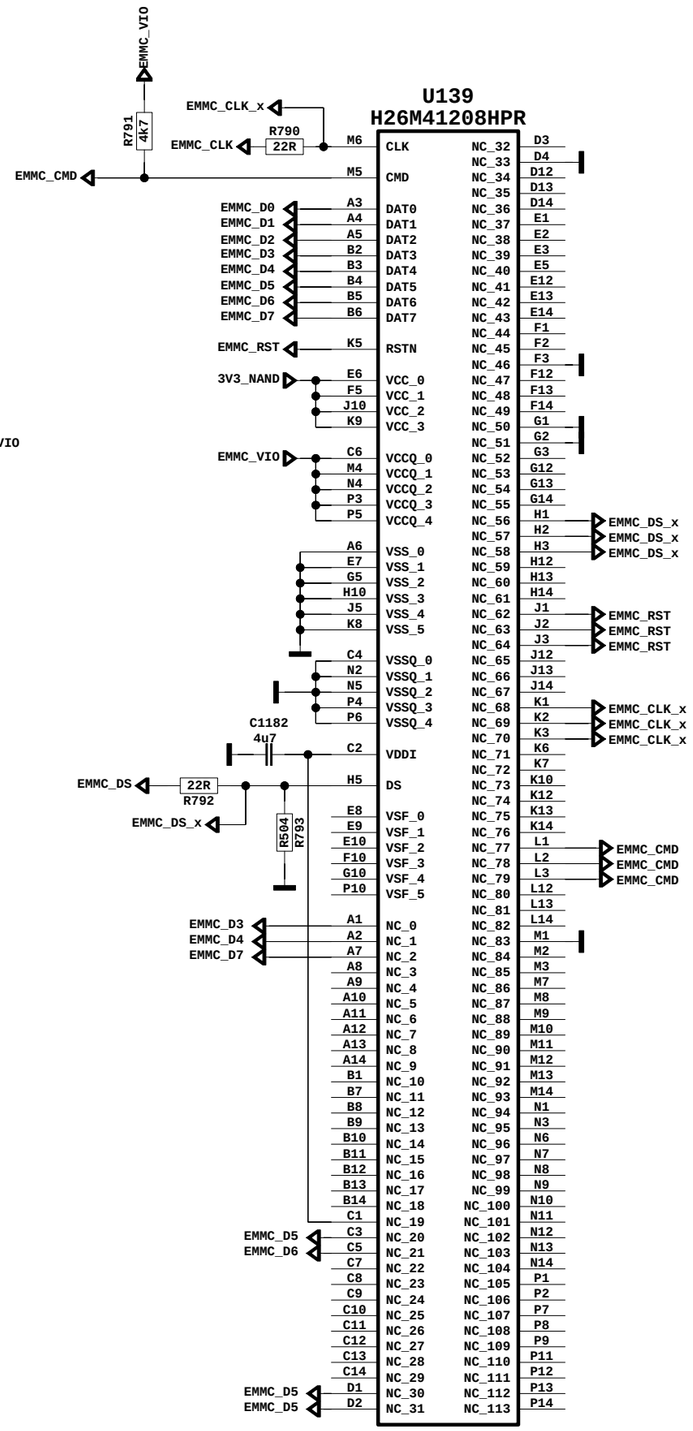


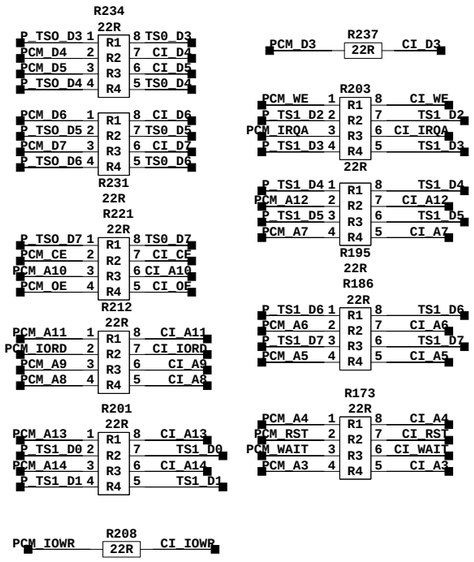
USB HUB

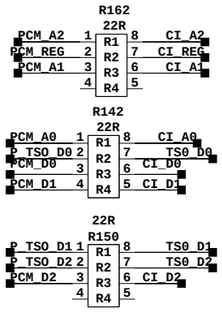












VESTEL	PROJECT NAME : 17mb181tc-r4	A3
SCH NAME :CI_NAND		T. SHT 11
DRAWN BY :<YOUR NAME HERE>		13/03/2020:09:37